RF Characterization of Square Spiral Inductors on a 0.25 μm Digital CMOS Process

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ABSTRACT

The growth of wireless applications in the low GHz range has been a catalyst in numerous research activities to develop wireless applications in standard digital CMOS processes. The relatively lower costs in developing single chip solutions for wireless applications in CMOS technology is considered its main advantage over other semiconductor processes. Thus, with the integration of RF systems in CMOS, planar inductors will have a dominant role in defining the achievable performance of the system as a whole.

The inductors used in this study were used in the input impedance matching for an LNA at 2.4 GHz. Plain square spiral inductors and square spiral inductors with Q enhancement structures are implemented on a 0.25 μm digital CMOS process with inductance values of 1.8 nH and 10 nH. On Wafer RF characterization of the inductors were done using an inductor model proposed by Yue. Results obtained show that parasitic resistance limits the Q of square spiral inductors on a digital CMOS process. Measured results also show how Q enhancement techniques reported in literature affect inductor Q on a digital CMOS process. It is recommended that shunted metals be used in improving inductor Q.

1. INTRODUCTION

CMOS is considered a technology of choice in the integration of RF systems in the low-frequency GHz range [1]. The continued downscaling of the NMOS transistor in CMOS processes has improved its characteristics adequately enough to be an attractive alternative for RF applications [2][3].

The integration of inductors in CMOS is a critical issue since it affects the performance of RF building blocks [4]. The quality factor of inductors in CMOS is limited by metal losses and substrate losses inherent with the technology. A recent publication in [5] has reported quality factors between 4 and 6 were achieved in a digital CMOS process.

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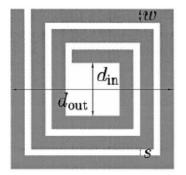
2. SQUARE SPIRAL INDUCTORS

Figure 1. Parameters to Describe a Square Planar Inductor [6]

Inductors implemented in Si technologies are fabricated using at least two metal layers. One layer is used to form the inductor structure and the other is used to bring the inner port to the outside using an underpass contact. A popular implementation of monolithic inductors is the square spiral inductor shown in Figure 1 because it is easy to generate using standard Manhattan based layout tools.

Figure 1 illustrates some of the parameters that define the effective inductance of a square spiral inductor. These parameters include the number of turns N, the metal trace width W, the spacing between metal traces S, the inner diameter d_{in}, and outer diameter d_{out}. Another parameter that affects the inductance is the metal thickness as discussed in [7] but is no longer considered in this study.

2.1. Inductance Calculation

Model	Expression for Inductance
Modified Wheeler Formula	$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}$
Current Sheet Approximation	$L_{gmd} = \frac{\mu n^2 d_{avg} c_1}{2} \left(ln \left(\frac{c_2}{\rho} \right) + c_3 \rho + c_4 \rho^2 \right)$
Data-fitted Monomial Expression	$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}$

Table I. Empirical Equations to Compute Effective Inductance

Empirical equations have been developed using the parameters discussed above in determining the inductance of spiral inductors [6]. These empirical equations are summarized in Table I and have been reported to have an error of about 3% as compared to the more computationally extensive 3D-field solvers. The values and definitions of the coefficients in each of the expressions are listed in [6].

2.2. Quality Factor

The quality factor, Q, for an inductor is given by Eq.1 [8]. It gives a quantitative measure of how much an inductor deviates from an ideal device.

$$Q = 2\pi \frac{|PeakMagneticEnergy - PeakElectricEnergy|}{EnergyLossInOneOscillationCycle} \qquad (1)$$

Based on this expression, Q can be improved by minimizing both electrical energy and energy losses. Electric energy is stored in parasitic capacitances in a spiral inductor while energy losses are attributed to resistive losses in the structure. The frequency when Q = 0 sets the self-resonant frequency for an inductor.

2.3. Induction Losses in CMOS

Losses associated with CMOS are generally classified into two: metal losses and substrate losses. Metal losses limit the realizable quality factor of inductors at lower frequencies, while substrate losses limit the quality factor at higher frequencies.

Metal losses are attributed to the resistivity of metal interconnects used in a digital CMOS process or the skin effect and other magnetic field effects that may cause a non-uniform current distribution in the inductor. Substrate losses are attributed to the heavily doped substrates in digital CMOS processes, which allow the generation of eddy currents leading to resistive losses in the substrate. These eddy currents also oppose the magnetic field produced by the coil.

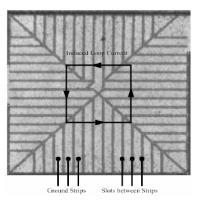## 2.4. Q-Enhancement Techniques

Figure 2. Patterned Ground Shield [8]

Q enhancement techniques fall under two categories: those that reduce ohmic losses and those that reduce substrate losses. Q enhancement techniques considered in this study are patterned ground shields [8], halo substrate contacts[9] and shunted metal layers[10]. The patterned ground shield and the halo substrate contact help isolate the spiral inductor from the substrate while the shunted metal layers are used to improve the conductivity of the metal interconnects. These structures are compatible with standard CMOS processes, and allow an

improvement in inductor performance without adding extra processing steps, which ultimately lead to higher costs [11].

By inserting a solid ground shield between the substrate and an inductor, eddy currents produced by the magnetic field of the inductor will induce eddy currents in the ground shield rather than in the substrate. To limit the effect of the induced eddy currents in the ground shield, the effective resistance of the ground shield should be increased. By inserting slots orthogonal to the spiral, as seen in Figure 2, the path for image currents is effectively removed. This is referred to as the patterned ground shield. The slots should be narrow however, so that the electric field generated by the inductor will not penetrate the substrate under the patterned ground shield. Effective grounding should be considered with the use of patterned ground shields. The ground strips should be merged in such a way that no loop path is produced under the spiral since this will lead to unwanted negative mutual coupling. Also, the merged strips should be connected to the top metal layer to reduce the resistance of the ground strips. The main objective here is to minimize the impedance to ground while preventing the generation of negative mutual coupling.

Another Q enhancement to minimize substrate losses is the use of halo substrate contacts [9]. The basic principle behind this method is the reduction of substrate losses by distributing ground connections around the planar spiral inductor to absorb the eddy currents produced by the inductors. Ground substrate contacts are provided along the periphery of the device to contain the RF signal flow. The introduction of ground contacts around the inductor should be provided through low impedance structures to minimize losses. Figure 3 clearly illustrates this structure. As with PGS structures, a closed loop path should be avoided when using a halo substrate structure, since this will cause unwanted negative mutual coupling that can reduce the effective inductance.
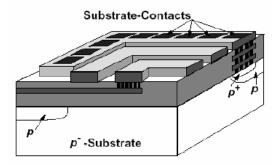

Figure 3. Halo Substrate Contact [9]

One way of improving the quality factor of spiral inductors is increasing the conductivity of the inductor by shunting several metal layers [10] as illustrated in Figure 4. This however has issues like how dense the via array should be to permit the shunting of metal layers [12] and the issue on how many metal layers is optimum [13]. As we increase the conductivity of the metal traces by effectively shunting several metal layers, the resulting resonant frequency decreases since the effective oxide capacitance of the inductor with the substrate is increased.
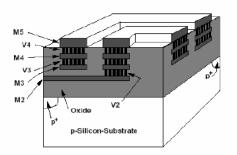
Figure 4. Monolithic Inductor using Shunted Metals [10]

3. IMPLEMENTED STRUCTURES

The inductors used for the input matching in a 2.4 GHz low noise amplifier were used [14]. The inductance values inductors are 1.8 nH and 10 nH. ASITIC [15] was used in the design of the inductors using the guidelines gathered from [4][5][16]:

- Width of inductor should be between 9-15 μm.
- A good inner radius should be 25% to 40% of the outer radius.
- Metal spacing should be as small as possible.

The inductors were implemented on a 0.25μm digital CMOS process. Table II summarizes the dimensions of the inductors implemented. Note that d_{in} was no longer measured since the listed parameters are adequate to define an inductor.

Inductance	Dimensions (μm)			
	N	W	S	d_{out}
1.8nH	3.5	10.88	4	160
10nH	5.5	9	4	275

Table II. Specification of Implemented Inductors

The different Q enhancement techniques considered in this paper were used for the 1.8 nH inductor. A combination of shunted metals and patterned ground shields were also considered to determine its effect on Q. However, only patterned ground shields and halo substrate contacts were used for the 10 nH inductor due to die area limit.

Each implemented inductor structure was placed in a test fixture with GSG probe pads for on-wafer measurements as shown in Figures 5 and 6.

4. MEASUREMENT AND MODELING

On-wafer measurements were conducted using a Micromanipulator Probing station, Microwave Probe Link Arms, GSG Picoprobes 40A-GSG-160-P, and an Agilent 8753ES Vector Network
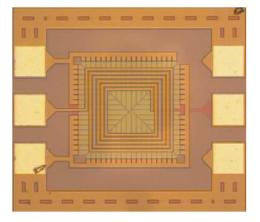
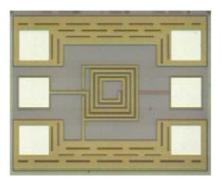Figure 5. 10 nH Spiral Inductor with PGS

Figure 6. 1.8 nH Spiral Inductor with Halo Substrate Contacts

Analyzer. The Short-Open-Load-Thru (SOLT) calibration was implemented using the Model CS-5 calibration substrate by GGB industries. Two port s-parameter measurements were conducted for a frequency range of 70 MHz to 6 GHz. Measurement quantities were then de-embedded using an open standard [17].

The model used to describe the behavior of monolithic inductors was presented by Yue in [18] and illustrated in Figure 7. In the figure, L_s models the inductance, R_s represents the resistance, and C_s represents the fringing capacitance. R_p reperesnets the shunt resistance and C_p represents the shunt capaciatnce. These model the substrate parasitics of the inductor. These parameters are easily derived from measured quantities using the flowchart shown in Figure 8. Each component value is computed per frequency point with $Z_o = 50$ ohms. Note that C_s was not determined from measured values since the self-resonant frequency of the branch containing C_s is beyond 6 GHz.
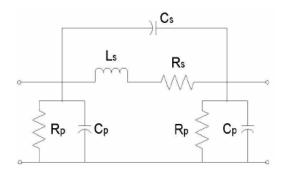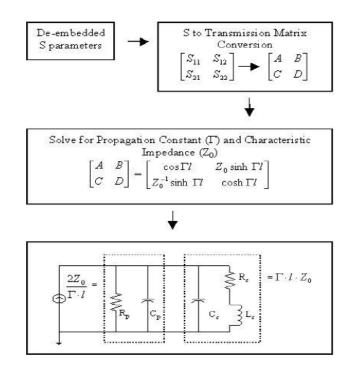
Figure 7. Yues Inductor Model [18]

Figure 8. Parameter Extraction by Yue [18]

5. DISCUSSION OF RESULTS

From results obtained, the use of different Q enhancement techniques did not affect the effective inductance for both 1.8 nH and 10 nH inductors. Shown in Figure 9 is the measured inductance for the 1.8 nH inductors. Looking at the extracted series resistance in Figure 10 for the 1.8 nH inductor, the use of shunted metal layers reduces the effective resistance of the inductor.

On the other hand, using either patterned ground shields or halo substrate contacts effectively increase the extracted series resistance due to image currents produced in these structures. The same results were also observed for the 10 nH inductors and is no longer shown.
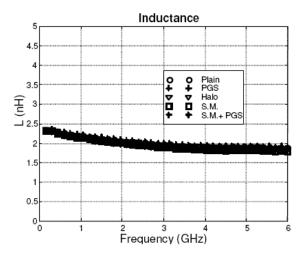

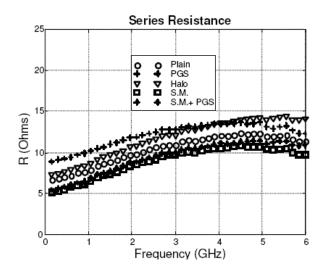Figure 9. Extracted Inductance for the 1.8 nH Inductors

Figure 10. Extracted Series Resistance for the 1.8 nH Inductors

The use of patterned ground shields contributes to an increase in the extracted shunt resistance. This verifies that ground shields are effective in reducing the substrate losses unlike for the halo substrate contact. This can be verified by looking at Figure 11 for the case of the

10 nH inductors. This was also observed for the 1.8 nH inductors. The shunted metal layer implementation had the lowest shunt resistance since this implementation places the inductor closest to the substrate thereby increasing the generation of eddy currents. Placing a patterned ground shield underneath slightly increases the shunt resistance for both the 1.8 nH and 10 nH inductors which demonstrates a reduction of eddy currents in the substrate.
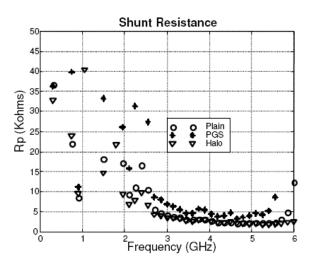

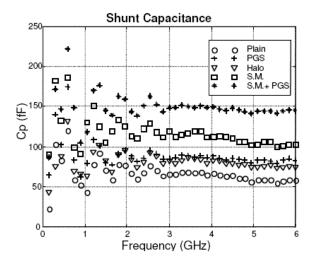Figure 11. Extracted Shunt Resistance for the 10 nH Inductors

Figure 12. Extracted Shunt Capacitance for the 1.8 nH Inductors

Figure 12 shows the summary of extracted shunt capacitance for the 1.8 nH inductor. The use of patterned ground shields contributes to higher extracted shunt capacitances. The

implementation with the highest extracted shunt capacitance is the combination of shunted metals and patterned ground shields. The use of shunted metals only is second in contributing a large shunt capacitance. For small inductors, the extracted shunt capacitance for inductors using patterned ground shields and halo substrate contacts are almost the same. For large inductors, the use of patterned ground shields contribute to higher shunt capacitances while using the halo substrate contact resulted in an almost equal shunt capacitance when compared with the plain inductor.
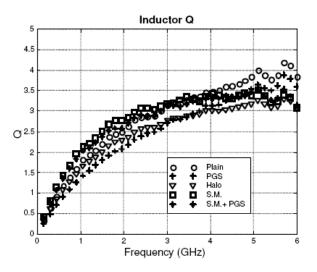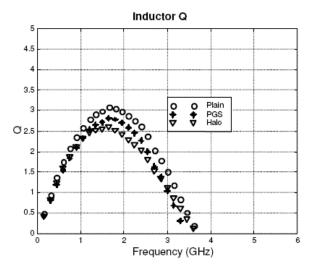
Figure 13. Extracted Q for 1.8 nH Inductors

Figure 14. Extracted Q for 10 nH Inductors

For the 1.8 nH inductor, the use of shunted metals has the greatest contributor in increasing Q for frequencies below 3 GHz. However, when frequency is increased above 3 GHz the substrate losses begin to dominate making the shunted metal technique ineffective. Looking at Figure 13, for frequencies above 4 GHz, using a plain inductor offers the best possible quality factor. The quality factor extracted from the inductor using patterned ground shields is better when compared with inductors using halo substrate contacts as seen in Figure 14. However, the high shunt capacitance associated with patterned ground shields reduces the inductors resonant frequency. It can be verified from the figure that the use of plain inductors gives the highest attainable quality factor.

6. CONCLUSIONS AND RECOMMENDATIONS

Extracted results show that using patterned ground shields and halo substrate contacts does not significantly improve the quality factor of inductors implemented in a digital CMOS process unlike in previous studies for bulk CMOS processes. It was determined that the use of these structures increases the effective series resistance since image currents are formed in theses structures leading to lower Q_s. Furthermore, results show that patterned ground shields offer better substrate shielding than compared to as can be seen from extracted shunt resistances. Shunted metal layers increase Q at the expense of a lower extracted shunt resistance thereby increasing substrate losses. The low quality factors of inductors observed should be considered in the design of RF circuits. For the target operating frequency of 2.4 GHz, inductors less than 10 nH should be considered due to the low Q_s obtained from this study.

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