

Analysis of Crack Propagation Under Different Die Tilt Configuration on a Small Outline Transistor

Jennifer F. Callanga¹, Hannah Erika D. Macaspac¹, Louis Angelo M. Danao¹, Manolo G. Mena²

¹Department of Mechanical Engineering, University of the Philippines, Diliman, Quezon City, 1101, Philippines

²Department of Mining, Metallurgical, and Materials Engineering, University of the Philippines, Diliman, Quezon City, 1101, Philippines

Abstract — *In today's microelectronic industry, the increasing demand for miniaturization and high function integration poses a big challenge in maintaining the reliability of the package. It was found out that majority of the reliability problems can be attributed to thermal and mechanical loadings during manufacturing and assembling process. Die cracking and die tilting are two of the most common defects originating from this process that affect the reliability of the electronic packages. This study aims to investigate the influence of die tilting to the propensity of crack propagation on the silicon die. In this research, the cooling phase of the die and clip attach reflow of small outline transistor was simulated using a finite element-based software. An initial crack was incorporated in the silicon die model to show the imperfections acquired during manufacturing stage. J-integral (J) parameter of fracture mechanics was employed as a criterion for the behavior of incipient cracks. With the assumption that the die used in this study exhibits linear elastic, isotropic property, the calculated J-integral values were correlated to the energy release rate (G). The simulation results showed that as the tilt angle increases, there is also a significant increase in the value of J-integral. The highest J value was observed on the maximum tilt angle. Moreover, this study presents clear relationship between the die strength and the specified failure factors; crack and tilt.*

Keywords — *Fracture Mechanics, ANSYS, Crack Propagation*

I. INTRODUCTION

In a power electronic system, power transistors are its most critical and integral component. As fundamental building block of modern electronic devices, its range of applications varies from household appliances, telecommunication, automotive, spacecraft power supplies, and virtually every aspect of human life [1].

As the demand for functionality and miniaturization increases, power transistors, such as Small Outline Transistors (SOT), are packaged as discrete yet high power density devices. Consequently, these SOT packages are exposed to harsher environment. They are subjected to higher temperature change and increased mechanical loadings like impact and vibrations. These conditions are often the cause of reliability problems, specifically thermo-mechanical, according to Zhang et al. [2]. Based from the same study, approximately 65% of microelectronic failures are due to or related to thermo-mechanical issues arising from the different stages of manufacturing process. One of the most common thermo-mechanical reliability problems is die crack. During the assembly process, packages are exposed to various temperature range and loading conditions. Knowing that these packages are multilayer and multi material, the response of each layer to the changes in temperature varies. The rate of

expansion or contraction differs for each layer due to the differences in coefficient of thermal expansion (CTE). These CTE mismatches cause thermal stresses in the package especially between different material interfaces. Accumulation of thermal stresses can create structural problem such as die cracking, and can aggravate initial defects in the package that can eventually lead to the package's failure.

Aside from die cracking, another reliability problem that can greatly affect the performance of an SOT package is die tilting. Die tilt happens when there is nonuniformity of the die bond thickness that causes the die to move or to incline in a certain direction. This reliability problem influences the package life by affecting the stress distribution in the die. [3]

Many studies were conducted to analyze the behavior of die cracking and die tilting. However, little (to none) has been involved in investigating the relationship of these two reliability problems. This paper aims to study the effect of different tilt angle on the stress distribution on the silicon die when exposed to temperature change during the cooling process of die-clip bonding. Moreover, it focuses on investigating the behavior of the crack and its propensity to propagate when subjected to various tilt configurations using finite element simulation coupled with fracture mechanics analysis.

II. FRACTURE MECHANICS BACKGROUND

The fracture mechanism of the die is due to two processes, crack generation and crack propagation. The first is due to extrinsic defects such as surface flaws, and the latter is because of the thermal loading that the package is exposed to. Cracks and flaws present in microelectronic packages may cause catastrophic failures when exposed to varying thermal loads and other external factors. To have the basic understanding of how crack propagates, fracture mechanics was established. Systematic rules have been developed to characterize cracks and their behavior.

2.1 Modes of Fracture Failure

Generally, a crack in a component has varying length and curvature. It is usually composed of two surfaces meeting at a common point or edge which is called the crack tip or crack front. The state of stress in the vicinity of the crack front varies from one point to another.

The basic mode of deformation and loading of the cracked component is shown in **Figure 1**. Mode I is the opening mode, and the displacement is normal to the crack surface. Mode II is sliding mode, and the displacement is in the plane of the plate where the separation is antisymmetric and the relative displacement is normal to the crack front. Mode III also causes sliding motion, but the displacement is parallel to the crack front, thereby, causing tearing. [4]

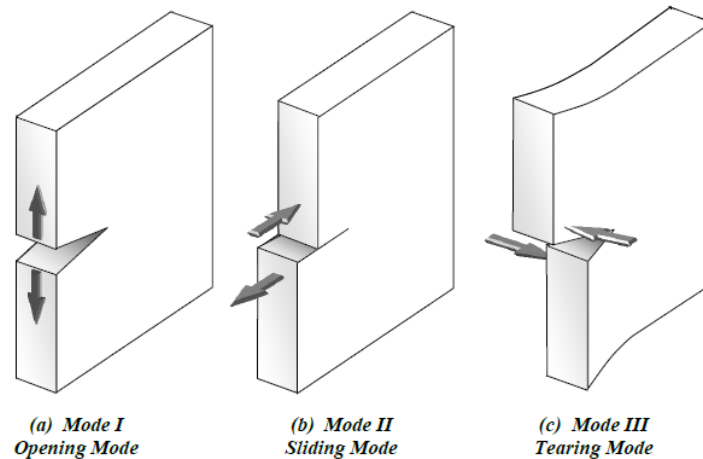


Figure 1. Three modes of fracture. [4]

Different parameters are used to characterize the crack in a component. One of the parameters is Energy Release Rate (G), which is energy based and is applied to brittle or less ductile materials. Stress Intensity Factor (K), on the other hand, is stress based, and is also developed for brittle or less ductile materials. The third one is the J-Integral (J). It has been developed to deal with ductile materials but is quite general and can also be applied to brittle materials. [4]

III. METHODOLOGY

In this study, ANSYS 15, a finite element-based software, was used to determine the stress distribution as well as the crack propagation behavior on the silicon die when subjected to different tilt angles. Furthermore, a two-step modelling approach was used to model the SOT package. A global model, which represents the full 3D package, was first generated and then a sub-model was created to where mesh refinement was done. Both global and sub models were drawn using ProE™.

3.1 Model Description

The SOT package used in this study is a multilayer structure consisting of different materials, namely silicon, solder, and metal alloy. **Figure 2** shows the geometry of the model. It has 4.13 mm x 3.53 mm silicon die bonded to a 4.5 mm x 4.68 mm copper leadframe using a 10 μm thick solder. The copper clip is attached on top of the die using a 75 μm solder.

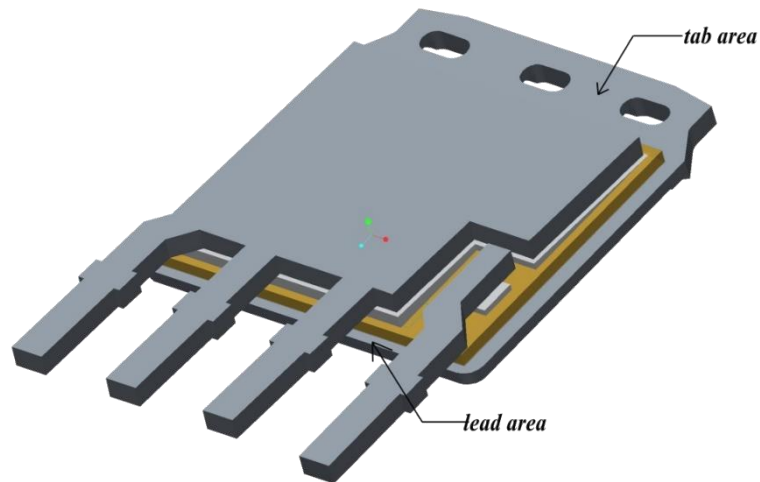


Figure 2. Clip and die assembly. [5]

For the sub-model, a technique called cut boundary displacement method was adopted. In this technique, the global response is evaluated first then the generated results are transferred to the local or sub model. The resulting displacements from the global model were applied to the sides of the sub-model as initial boundary conditions. In this research, the sub-model as shown in **Figure 3**, is composed of the same five components with the global model, and has a dimension of 200 x 200 μm .

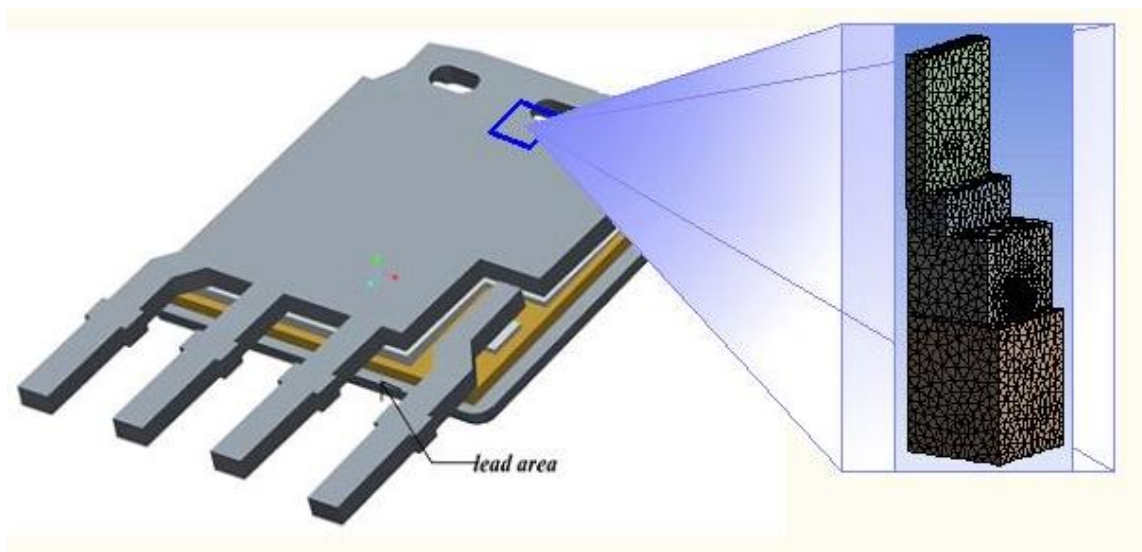


Figure 3. Sub-model of the package

For simplicity, the materials used in this study are assumed to be linear elastic and isotropic. The detailed material characteristics of the SOT packaged is shown in **Table 1**.

Table 1. Elastic properties of SOT materials [5]

Material	Young's Modulus (GPa)	Poisson's Ratio	CTE(ppm/C)
Silicon Die	169.00	0.23	3.0 (100)
Clip	120.00	0.35	17.7
Leadframe	120.00	0.35	17.7
Solder	26.00 (-65°C)	0.4	13.3 (-65°C)
	16.93 (260°C)		9.2 (150°C)

3.2. Thermo-mechanical Set-up

In doing the thermo-mechanical simulation, the SOT package was exposed to a temperature of 370 °C, which is the die and clip attach reflow temperature, and was cooled down to room temperature of 25 °C. At the start of the simulation, the package was assumed to be in a stress-free condition. Usually, the stress-free temperature is set at the melting point of the die attach material.

To avoid the rigid body motion, the fixed point in the package (all DOF are constrained to zero) was set to be the right most bottom corner of the copper leadframe. Other corners were constrained to move in y directions. [6]

3.3 Die Tilt Modelling

In this study, the effect of die tilt angle on the behavior of the crack was investigated. Both the upper and bottom solder tilts were modeled and analyzed. Die tilt here was defined by the vertical displacement of the silicon die, and is measured along the lead area.

The bottom solder, which is designated as the layer between the leadframe and the silicon die, measures 10 µm thick. For this simulation, three tilting cases were tested. The tilt was oriented in such a way that the thinner side is along the tab area, as shown in **Figure 4**. The maximum measured tilt angle was 0.32°, which corresponds to a die's vertical displacement of 20 µm.

Table 2. Tilt angle values for bottom solder

Case Number	Tilt Angle
1	0.00°
2	0.16°
3	0.32°

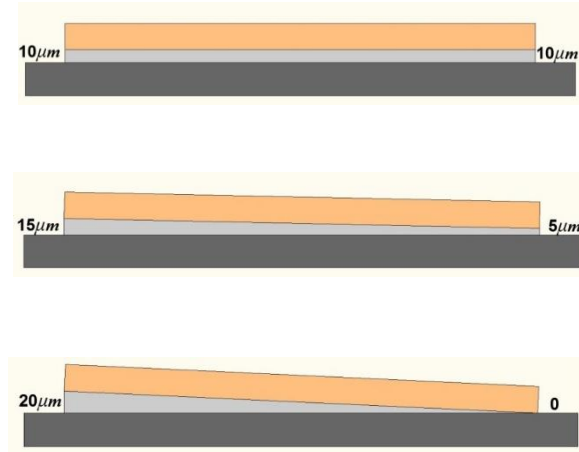


Figure 4. Bottom solder height variations

On the other hand, the layer between the silicon die and the copper clip is what referred here as the upper solder. Only the solder below the larger clip was tilted. This set-up is shown in **Figure 5**. Same with the bottom solder, three tilting cases were also tested. The first case is a no tilt case. In this case, the solder is uniformly distributed and the top surface is flat. The third case is the worst case. Here, one edge of the clip is touching the silicon die surface. For the upper solder, the maximum tilt angle is around 2.57° . Note that in this simulation, it was the clip's angle that varies. The silicon die remains flat for all five cases. The mesh set-up and boundary conditions applied to the bottom solder were also used in this simulation.



Figure 5. Upper solder tilt angle variation

3.4. Crack Formulation

In order to model, create and formulate the crack, the ANSYS software was again used. This semi-circular crack was introduced as a defect on the free side of the sub-model. This crack is usually acquired during initial processing such as sawing, grinding or transferring of die. According to the study conducted by D. F. Calvez, et al. [7], the typical crack length size is around $2 - 3 \mu\text{m}$. In this paper, the $3 \mu\text{m}$ limit was utilized. The defect was oriented vertically

from the bottom and was run upwards. The crack was drawn as close as possible to the edge to model the actual scenario as shown in **Figure 6a and 6b**. Refinement was done on the sub-model to properly model the embedded crack. To be able to account for the crack tip stress singularity in the induced defect, a tetrahedral mesh with size of 0.0005 mm was used.

The crack propagation in the sub-model was analyzed using fracture mechanics. There are three parameters used to characterize the crack: J-integral (J) that is based on the integral domain approach, stress intensity factor (K) that is calculated through displacement extrapolation, and energy release rate (G) that is derived from virtual crack closure technique. [4] J-integral method was used to describe the behavior of the crack in this research. J-integral calculation is applicable for linear elastic, nonlinear elastic and elastoplastic materials.

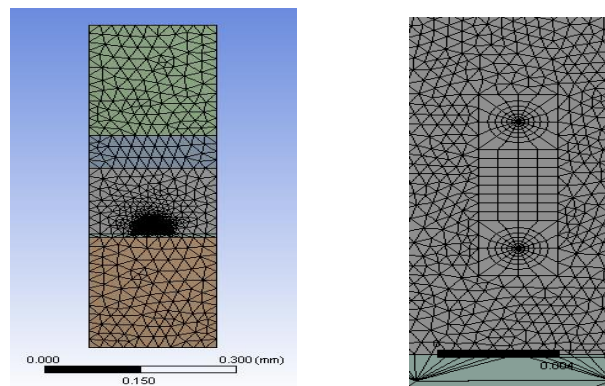


Figure 6a. Sub-model with crack **Figure 6b.** Schematic of crack

For linear elastic materials, J-integral is equal to the energy release rate as described in Eq. 1,

$$J = G = - \left(\frac{\partial U}{\partial a} \right) \tag{Eq. 1}$$

where ∂a is the length of the new crack and ∂U is the potential energy available for crack to grow. [4] Based from the assumption made in the previous section where silicon die was modeled with linear-elastic isotropic property, the J-integral values calculated from the simulation can be correlated to the energy release rate (G). J-integral is related to the stress intensity factor, K , using **Eq. 2**. [8]

$$J = G = \frac{1 - \nu^2}{E} (K_I^2 + K_{II}^2) + \frac{1 + \nu^2}{E} K_{III}^2 = \frac{1 - \nu^2}{E} K^2 \tag{Eq. 2}$$

where the subscripts I and II denotes the failure modes and E is the Young's modulus. The stress intensity factor calculated from the J-integral method will be compared to the critical

fracture toughness K_c of silicon for $\langle 111 \rangle$ plane. The K_c of a material is obtained through experiments. When the value of K obtained from the J-integral formula, is greater than the K_c it means that the crack propagation will commence.

IV. RESULTS AND DISCUSSION

A finite element model was constructed to investigate the effect of tilt angles on the stress distribution as well as the crack behavior on the SOT package. Three tilt configurations of top and bottom solder were applied to the model.

4.1 Effect of Tilt to Stress Distribution on the Die

For the first part of the analysis, the maximum principal stress failure criterion was used. This criterion is often used to determine whether a brittle material will fail or not when subjected to severe loadings.

Figure 7a shows the maximum principal stress distribution on the die due to upper solder configuration. For this configuration, the maximum stress is located on the upper right corner of the tab area. As the tilt increases, the maximum principal stress distribution shifted to the thinner side. It can also be observed that the stresses in the die where the thinner side of the solder is located, increases with increasing tilt angle.

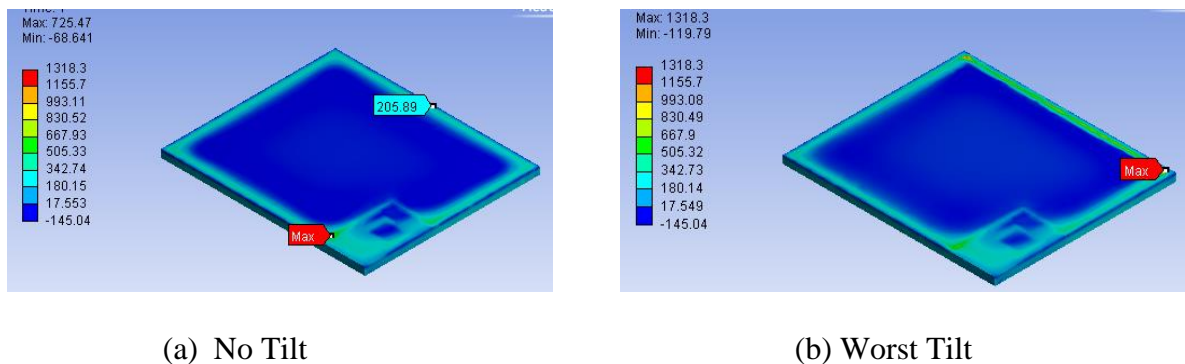


Figure 7. Maximum stress distribution on the die due to upper solder tilt [5]

For the bottom solder tilt, it can be observed from **Figure 8** that as the tilt angle increases, the principal stress distribution from the lead to the tab area also increases. However, the highest value of principal stress was found to be located at the lower right section of the lead area. This area, as shown in **Figure 2**, is where the clip and the surface of the die meets. Thus, this value could be attributed to the geometrical discontinuity of the package.

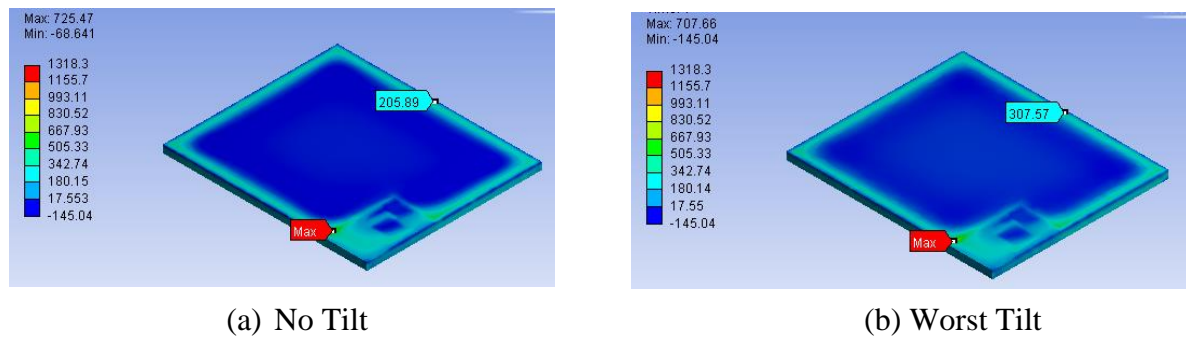


Figure 8. Maximum stress distribution on the die due to bottom solder tilt [5]

The thermo-mechanical simulation results showed that when a package undergoes cooling process, the interface between the die and solder are the most stressed areas. This indicates that more attention should be given to these locations in the design process.

One important observation from the simulation process conducted in this study was that the value of the maximum principal stress does not converge even when fine mesh was used. Also, the location of these maximum stresses is usually at the corners or at the area where there is a sudden change in the geometry. Based from the study of the mechanics of materials, these corners represent stress singularity points. These are the areas where stresses tend to be of infinite values. Given this fact, it is difficult to compare stress values and doing so could lead to wrong results. Thus, in this study, the thermo-mechanical simulation based from conventional finite element method (FEM) was only used to observed the stress distribution on the silicon die when subjected to varying tilt angles, and not to use the maximum stress value as determining parameter on whether the die will fail or not.

4.2 Fracture Mechanics Analysis Results

Given the limitation of the conventional finite element method, fracture mechanics analysis was employed. Based from the results of the thermo-mechanical simulation, the maximum principal stress tends to shift to area where the thinner solder is located. For this study, it was set at the tab area. Thus, in doing the fracture mechanics simulation, the crack was placed on this side of the silicon die. Also, this location coincides with the actual crack location on the damaged SOT package. The actual damaged SOT package was used as reference in this study. In the actual package, the crack originates from the die back side and propagates to the top surface.

In order to characterize and analyze the crack behavior, J-integral fracture criterion was used. As stated in the previous section, J-integral can be equated to energy release rate for elastic material. Using the relation between J and K , the fracture toughness in each tilt configuration can be computed. The computed K was then compared to the critical fracture toughness, K_C of silicon which is around $0.83 \text{ MPa}\cdot\text{m}^{1/2}$. [9]

4.2.1 Effect of Bottom Tilt to Crack Propagation

From **Table 3**, it can be observed that for the bottom solder tilt, the value of J-integral increases with the tilt angle. Also, all the computed K s are below the critical fracture toughness. This shows that at the given crack length and crack location, the energy on the crack is not enough to make it propagate.

Table 3. Values of J-integral for different bottom solder tilt

Tilt Angle	J-integral ($mJ.mm^2$)	Computed K ($MPa.m^{1/2}$)
0.00°	0.0048248	0.43
0.16°	0.0066732	0.60
0.32°	0.0076857	0.69

4.2.2 Effect of Upper Solder Tilt to Crack Propagation

The effect of upper solder tilt to the crack propagation was also evaluated. Based from the simulation results in **Table 4**, the J-integral value at no tilt case is almost twice than that of the worst case tilt. Although the values do not show some trend, it can be noticed that none of the computed K s is higher than the critical value.

Table 4. Values of J-integral for different upper solder tilt

Tilt Angle	J-integral ($mJ.mm^2$)	Computed K ($MPa.m^{1/2}$)
0.00°	0.0048248	0.4305
0.16°	0.0062549	0.5581
0.32°	0.0041939	0.3742

Based from the results of the simulation, die tilt due to uneven distribution of either upper or bottom solder will not cause crack propagation in the die even in the worst tilted case. However, it can be seen from Figure 9 that the trend of stress intensity factor caused by bottom solder tilt is increasing. It can be assumed from this, that somewhere along the succeeding process, after die attach, the value K of the package can go beyond critical K . This means that the initial crack will propagate and will eventually lead to die cracking.

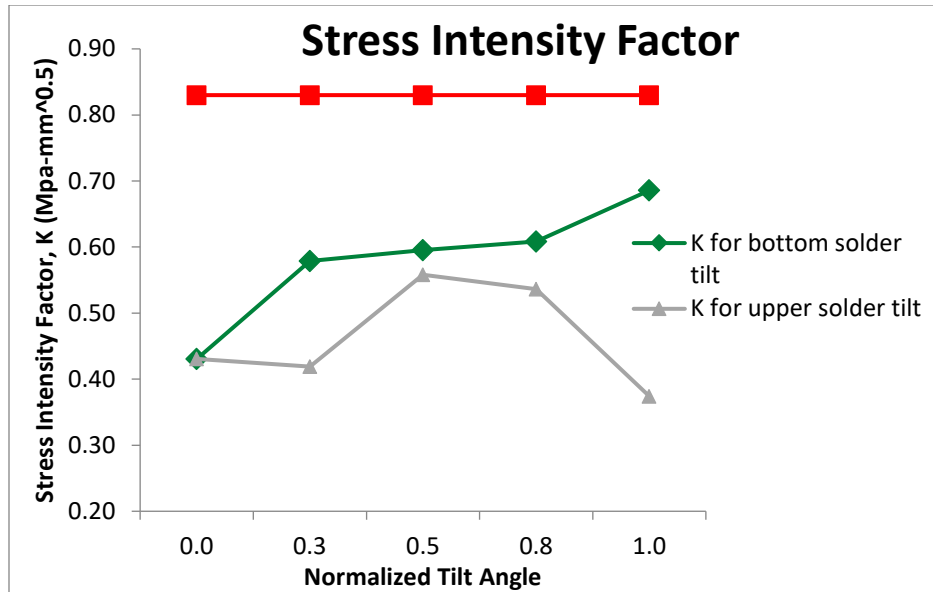


Figure 9. Stress intensity factor, K vs. Fracture toughness, K_C .

4.2.3 Stress Intensity Factor and Compressive Stress

Materials can fail in three different modes. It can fail through crack opening (Mode I), by sliding (Mode II), or by shear (Mode III). Most of the brittle materials fail by Mode I fracture. In this study, it is impossible for the die to fail by Mode I since most part of the die experienced a compressive stress. This is because of high CTE mismatch between the die and the leadframe. As the temperature goes down, the material with higher CTE contracts more compared to the one with lower CTE. In this study, the die has only 2×10^{-6} CTE while the leadframe has 17.7×10^{-6} . Thus, the die will contract less compared to the leadframe. **Figure 10** shows that the maximum compressive stress at different tilt angles, is on the bottom surface of the die where the initial crack was located. It can be observed that in that part of the die, the distribution of compressive stress becomes more concentrated towards the center. The maximum compressive stress for the worst tilt case for both upper and lower solder is located on the corners where the solder is the thinnest. As the tilt increases, the value of compressive stress also increases. This can be seen in **Figure 11**, where K_I becomes more negative as tilt angle increases.

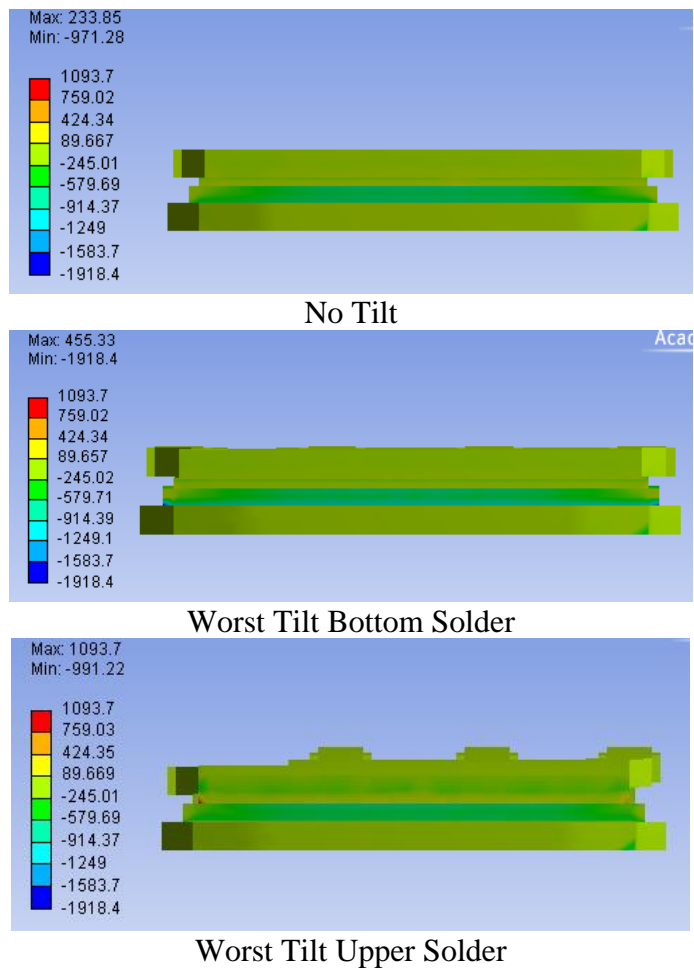


Figure 10. Compressive stress distribution in the die

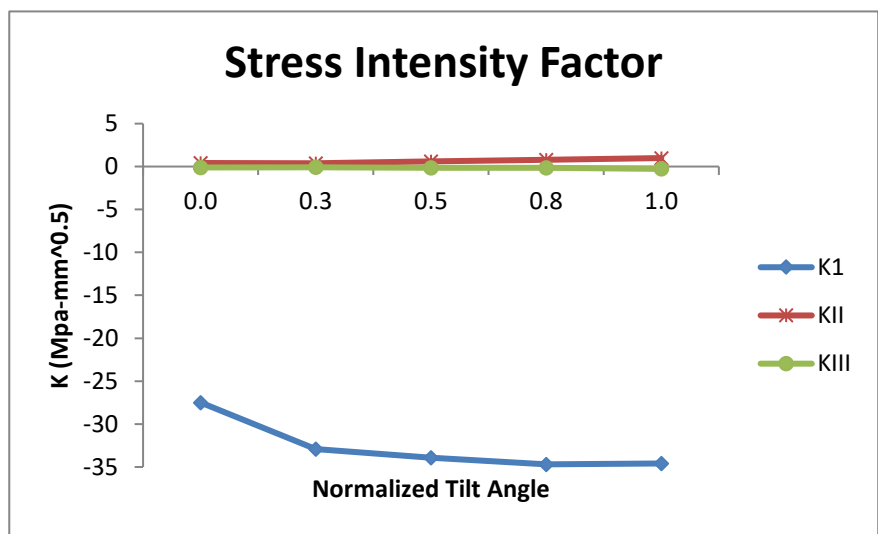


Figure 11. Stress Intensity Factors for the Bottom Solder

V. CONCLUSION

In this research, thermo-mechanical simulations were conducted for multilayer SOT package to assess its thermal behavior. It was coupled with fracture mechanics approach to investigate the impact of die tilt to crack propagation.

The impact of tilt angle on the thermo-mechanical behavior of the package is significant in terms of determining the most stressed area. The stress distribution on the die shifted to the side where the solder is the thinnest as the tilt angle increases.

The effect of varying tilt angles on the behavior of the crack was also studied. The J-integral method was used to quantify the amount of energy available in the crack. Based from the results, the J-integral increases with increasing tilt angles. The J-integral for the worst tilt case of the bottom solder is 13% higher compared to the no tilt case. While for the upper solder tilt, the J-integral values for worst tilt case is almost negligible compared to no tilt. No values of J-integral, for both upper and bottom solder, exceeded the critical value.

Based from the results, it can be concluded that varying tilt angle of both upper and bottom solder has little effect to the behavior of the crack in the package. For the given crack length and crack location, tilt angle won't cause crack propagation.

The results of this study are limited to the SOT package configuration and crack characteristics used. For future studies, it is recommended to investigate the effect of other crack parameters such as crack length, crack orientation and crack distance from the edge to better characterized the crack behavior.

NOMENCLATURE

a	length of new crack (mm)	SOT	Small Outline Transistor
c	critical	U	Potential Energy
CTE	coefficient of thermal expansion		
DOF	degrees of freedom		
E	Young's Modulus (GPa)		
FEM	Finite Element Method		
G	Energy Release Rate (mJ-mm ²)		
J	J-integral (mJ-mm ²)		
K	Stress Intensity Factor (MPa.m ^{1/2})		
			<i>Greek Symbols</i>
		∂	change in the parameter
		ν	Poisson's Ratio
			<i>Subscripts</i>
		<i>I,II,III</i>	Failure modes

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