Investigation of Silicon Die Crack for Varying Silicon Die Parameters and Die Attach Material

Hannah Erika D. Macaspac[1], Jennifer F. Callanga[1], Richard Raymond N. Dimagiba[1], Manolo G. Mena[2]
[1]Department of Mechanical Engineering, University of the Philippines, Diliman, Quezon City, 1101, Philippines
[2]Department of Mining, Metallurgical, and Materials Engineering, University of the Philippines, Diliman, Quezon City, 1101, Philippines

Abstract— *Demand for small sized, portable electronic devices continually increases until today. Compact electronics would mean a reduction in size of semiconductors that would translate to further shrinking of components inside of it such as the small outline diode (SOD) and the small outline transistor (SOT). This work utilized the finite element method with a fracture mechanics approach to analyze the effect of varying geometric parameters on the J-integral of an induced crack on the silicon die. Furthermore, investigation of the effect of two die attach materials, having different modulus of elasticity, on the crack propensity on the silicon die was done. The J-integral values obtained generally showed a peak value with the mid-sized silicon die whose die attach material has higher modulus of elasticity. The J-integral value generally decreased with die thickness but was found to be minimum at around 100 mm die thickness. A further reduction in thickness resulted in an increase in J-integral. Results from the simulations will aid in determining the effect of these parameters on the reliability of the package with respect to die crack risk and can be utilized to guide improvements on the existing package design.*

Keywords—die crack, J-integral, small-outline transistor

I. INTRODUCTION

Miniaturization in electronic devices was introduced since the World War II and continues to be a trend until today. The demand for small-sized, portable electronics has advantages such as higher speed and reduced cost. Smaller electronics, due to closely packed components, make signals travel less distances within the device avoiding delays [1]. Electronic devices are made of semiconductors connected to each other. These semiconductors have a wide range of applications in telecommunication, automotive, and mobile systems that demands miniaturized electronics and sensors [2]. Compact electronics would mean a reduction in size of semiconductors that translates to further shrinking of components inside of it such as the small outline diode (SOD) and the small outline transistor (SOT). Consequently, parts of the SOD or SOT such as the dies should also become smaller and thinner in order to fit in a smaller area.

Due to the size reduction of individual components inside the SOD or SOT, special attention should be given in their handling. Silicon die, which is the heart of the SOD and SOT is a brittle material which makes it prone to rapid propagation of fracture [3]. Cracks, or in more severe cases, fracture could result if a load is incorrectly applied to it causing unnecessary stresses. While the reduction of silicon die sizes may be advantageous, the geometry might affect its strength if subjected mechanical or thermal loads.

Studies have been conducted on how die geometries affect stresses in microelectronic packages. Yuning Shi [4], Michaelides et al. [5], and Chong et al. [6] have conducted studies on the effect of die thickness and die size changes on the stresses experienced by the silicon die. Results obtained from their studies however vary due to the difference in the range of the thickness and size they utilized. Different combination of materials and geometries would lead to different result trends. In addition, the aforementioned studies only showed the effects of the parametric changes on the silicon die on its strength. The assumption was that the silicon die does not include defects which is not the case in actual applications.

Several studies have also been conducted on silicon die cracking. Studies made by Calvez et al. [7] and Mercado et al. [8] showed how the coefficient of thermal expansion (CTE) and the Young's modulus affect the silicon die edge cracking. These two factors are both properties of a material that would greatly affect the behavior of material especially on thermal loadings.

In order to avoid die cracking, which may lead to the failure of the package component, SOD or SOT assembly should be done carefully. At the early stage of the assembly, possible location of maximum stresses should be determined in order to monitor the state of the component as they undergo the assembly process. This entails assembly of minute components to test certain parameters on the package to ensure reliability, which will be difficult to set up due to its size and the volume of components needed to be manufactured. Finite element analysis (FEA) therefore becomes very useful in simulating conditions for the analysis of packages with small sizes.

This study aims to utilize FEA in the investigation of the effect of varying silicon die parameters and die attach material on the induced stress and crack response under thermal loading, specifically, for 3.2mm x 4.00 mm, 2.2mm x 2.7mm and 1.2mm x 1.7mm silicon die sizes and for 100 μm and 200 μm silicon die thicknesses. The propensity of the crack to propagate is then evaluated using the fracture mechanics approach. The results of the FEA and the fracture mechanics approach are used to determine which geometric parameter combination in the small outline transistor (SOT) will give the lowest risk of crack propagation.

II. METHODOLOGY

2.1 Model Description

A small outline transistor, as shown **Fig. 1**, is usually composed of the leadframe: the base of an electronic package; silicon die: considered as the heart of an SOT; wires: connect the silicon die to the leads, which connect to the circuit board; die attach material: attaches the components to each other and provides support between the silicon die and the leadframe; and the encapsulant which covers the whole package. The focus of this study is the cooling after the die attach process; therefore, only the leadframe, solder and silicon die will be utilized as illustrated on **Fig. 2**.

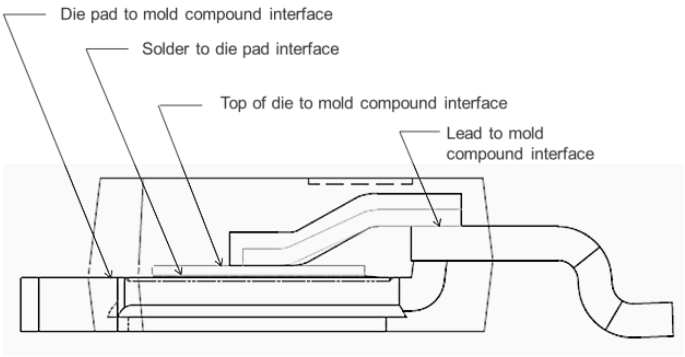

Fig. 1: 2D model of a wire-bonded SOT package

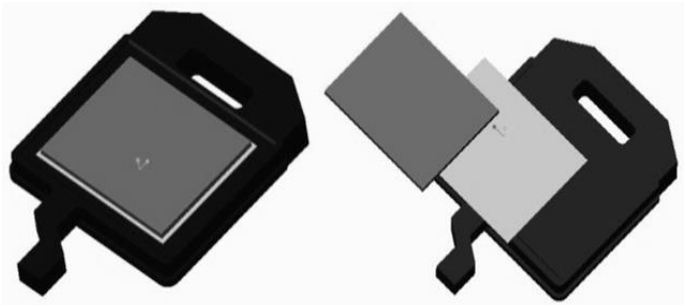

Fig. 2: 3D Model of the SOT package used in the simulation

The reason of utilizing only three SOT components is that based on a study on packaging assembly, the die attach process has the highest temperature requirement among all other process that a package goes through. During the process of die attachment, the temperatures that the package may experience ranges from 260ºC to 345ºC [9]. During the aluminum wire bonding process, according to Pan and Freud [10] , temperature can range from room temperature to 220ºC. The molding and the curing of the epoxy molding compound used on the package happens at a temperature of 175ºC [11]. Given these temperature ranges, processes occurring after the die attach can therefore be neglected since stresses that will be obtained from them will be less than the stresses after the die attach process.

2.2 Model Generation

A 3D modelling software Creo Parametric 2.0 was used to generate the wire bonded SOT package illustrated in **Fig. 2**, with only three components – the leadframe, solder and silicon die. Components that were unnecessary in the simulation such as the wires and encapsulant were not included in the model generation.

Six assemblies were generated for geometry changes in the simulation. Die and solder sizes were varied while maintaining an aspect ratio (L/W) of 0.8. Thickness of the silicon die was changed, as well, from 200 μm to 100 μm. The dimensions of other components were not varied, the leadframe's and solder's thickness remained the same at 0.8mm and 0.3mm, respectively.

In addition to the changes in the geometry, two variations of assemblies were done to capture the changes in die attach material resulting to twelve geometry simulations. **Table 1** shows the dimensions of the silicon die used for the simulations.

TABLE 1. Silicon Die Dimensions

Assembly	Length (mm)	Width (mm)	Aspect Ratio	Thickness (µm)
Assembly 1	3.2	4.0	0.8	200
	3.2	4.0		100
Assembly 2	2.2	2.7	0.8	200
	2.2	2.7		100
Assembly 3	1.2	1.5	0.8	200
	1.2	1.5		100

2.3 Material Assignment

An essential part in any simulation is the assignment of materials as this will lead to the proper behavior simulation of a component. In this study, the behavior of the SOT package experiencing thermal loads during actual package cooling was simulated.

Determination of induced stresses on the package was done using a static structural simulation carried out in ANSYS Workbench 16.0 after the model was imported. All components were modeled as isotropic elastic materials. Both thermal and mechanical properties of each material used in the package are listed in **Table 2**.

TABLE 2. Material Properties

Material	Young's modulus (GPa)	Poisson's ratio	CTE (1E-6/K)	Density (g/cm^3)	Liquidus Temperature (ºC)	Solidus Temperature (ºC)
Copper leadframe	120	0.35	17.7	8.90		
Die	169	0.23	1.00 (-100 ºC) 2.35 (0 ºC) 3.10 (100 ºC) 3.50 (200 ºC)	2.33		
Die attach1	23.33 (25 ºC) 21.78 (80 ºC) 20.52 (125 ºC) 19.82 (150 ºC)	0.40	29.0	11.02	296	287
Die attach 2	13.01 (25 ºC) 9.79 (80 ºC) 7.16 (125 ºC) 5.69 (150 ºC)	0.40	28.8	11.20	304	299

2.4 Boundary Conditions

Necessary constraints in the model were assigned to properly simulate the conditions in actuality during the cooling process after the die attach. The boundary conditions used for the package include one fixed support, and three displacements assigned to different corners in the leadframe. This was done to restrict them from moving unnecessarily in the x-, y- or z-directions. The top and bottom views of the boundary conditions assigned to the model are shown in **Fig. 3**.

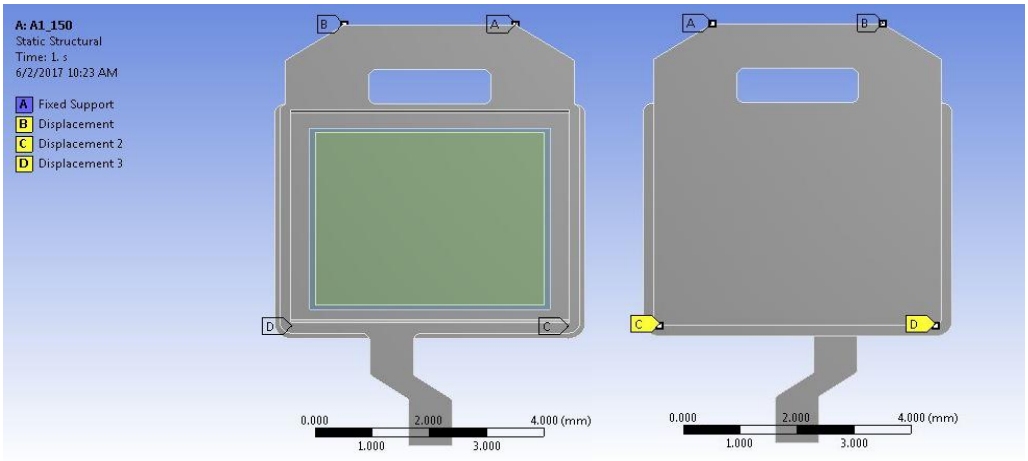

Fig. 3: Top and bottom view of the boundary condition

2.5 Mesh Density Study

When assigning the number of elements in a mesh density, it is desired to have sufficient refinement without compromising computing time. A fine mesh is generally used since, in theory, it can give the best approximation of the solution.

This study used the mesh refinement technique wherein meshes were done for the model, one being finer than the previous mesh. A total of three meshes were done for the whole SOT package, with 0.1mm, 0.05mm and 0.025mm element sizes for both the solder and silicon die. The three initial meshes done were observed to have non-converging maximum principal stress values with locations changing with every mesh. A finer mesh was therefore needed to be generated until the location of the maximum principal stress became stable.

Finer mesh requires more simulation time and larger computer memory. Due to the computer memory constraint, further mesh refinement was not possible. A body sizing of 0.025 mm for the silicon die and solder on the whole SOT package was the smallest element size that can be run. One solution to the problem is to create a submodel that would refine only the parts of the geometry that is problematic. In the model, since the focus was determining die cracks, the generated submodel consists only the silicon die where the maximum principal stress occurs for element sizes 0.05mm and 0.025mm.

Six additional mesh refinements were done on the silicon die from 0.01875mm up to an element size 0.0125mm. The number of elements was approximated to be around 1-4 million, from the first refinement up to the last. Significant changes in the maximum principal stress values were still observed as the element sizes were reduced. The location of the maximum principal stresses, on the other hand, was observed to be on the same position, at the upper left corner of the silicon die, for all the finer meshes. The stable location of the maximum principal stress indicates that further mesh refinement, if necessary, and analysis should be done only on that portion of the silicon die as this is where failure most likely to occur.

2.6 Submodel Creation

From the mesh refinement study, it was observed that the location of maximum principal stress became consistent in the upper left corner of the silicon die as the mesh of the package is refined. A sub-model was therefore created on the portion of the silicon die experiencing the maximum stress.

To properly simulate the component's condition in actuality, a crack was induced on the silicon die. There are two types of cracks that usually occurs in dies— the horizontal, and the vertical cracks [8, 12]. Between the two, horizontal crack, which moves inwards from the die edge, is more often observed. This kind of crack is usually caused by the singulation process or wafer dicing process. It was therefore necessary to induce a horizontal crack in the model.

The horizontal crack generated on the upper left corner of the silicon die, as shown in **Fig. 4**, was a way of checking if a failure might occur in the package. The study made by Yuning Shi et al. [7], and Calvez et al. [13] found that the usual size of a crack occurring on the silicon die is around 2-3μm. Given this crack size, a submodel was made to be large enough to fit the crack.

The placement of the submodel was also essential to determine the stresses occurring in that small portion of the silicon die. Proper location of the coordinate system of the submodel will determine the correct stresses relative to the whole model. A submodel with a 0.1 mm x 0.1 mm x 0.04 mm dimension was then generated, positioned at the upper left corner of the silicon die and just above the solder, where the maximum principal stress occurred during the mesh refinement.

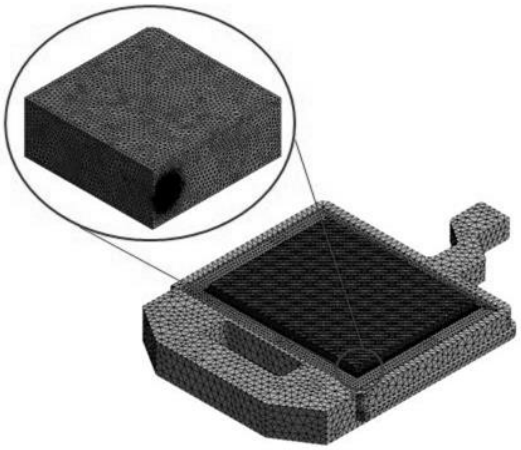

Fig. 4: Submodel

In the submodel mesh, a fine global mesh was used in order to have the right mesh for the crack model. Body sizing sphere of influence was also employed to ensure that only the bodies within the sphere will be affected by further mesh refinement. This method will save time and computer memory. Furthermore, a tetrahedron meshing method was applied to the model in order to allow for crack generation. Other meshing method like the quadrilateral meshing method would not allow generation of cracks in the model.

2.7 Fracture Model

The crack initiated on the upper left corner of the die, as seen on **Fig. 5**, represents the die edge defects brought about by the manufacturing of dies. The presence of the initiated crack and the corners in the bonded materials' interface in the model causes stress singularities. A simple stress analysis will therefore not suffice, to compute for the stresses [8, 14, 15]. A fracture model was deemed necessary.

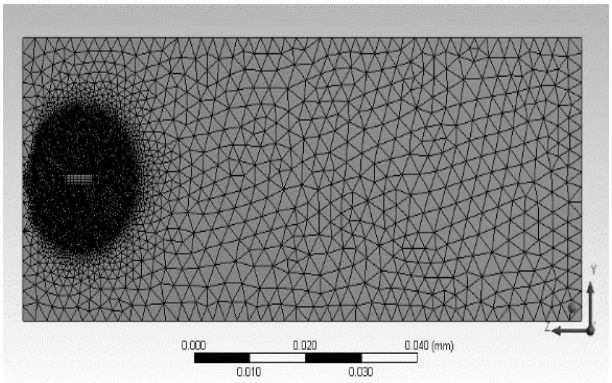

Fig. 5: Silicon die submodel

In this study, the 3 μm crack size was used to obtain the J-integral at the extreme condition. The J-integral is a path independent failure criterion that is used for the computation of the energy flow to the crack tip to estimate the crack opening [16]. A semi-circular crack was generated on the face of the silicon die where the maximum principal stress was observed

from the mesh refinement. The location of the crack was positioned as close to the edge of the silicon die as possible and at the middle of the silicon die thickness. Crack geometry refinements were also done to determine the crack geometry that can give solutions without having to run longer simulation and will not necessitate significantly more memory.

2.8 Thermo-mechanical Analysis

After all the parameters were set, the thermal condition of the cooling after the die attach process was simulated and was applied to the whole model and the submodels. The package was made to cool down from melting temperatures of the die attach materials to a room temperature of 25°C. The melting temperature of the die attach materials is at 294°C and 304°C for the die attach 1 and 2, respectively. The melting temperatures are considered the stress-free temperature of the model. A total of 12 simulations were made to get the J-integral for each model with every change in die size, die thickness and die attach material.

III. RESULTS AND DISCUSSION

The focus of this study was to evaluate die crack possibility with varying die size, die thickness and die attach material on a SOT package. Studies have shown that changes in these parameters greatly influence cracking on the silicon die. In this work, finite element analysis was done to obtain the J-integral of the silicon die crack with these varying parameters. The J-integral values obtained from the simulation was used to indicate if a package would fail due to cracking on the silicon die. The analysis of results was based on the cooling stage of the SOT package from its melting temperature to a room temperature of 25^{o}C.

3.1 Maximum Principal Stress

Maximum principal stress is usually employed for brittle materials to check for fracture. If the maximum principal stress exceeds the ultimate tensile strength of the material, fracture will occur. Silicon die in the package is a brittle material; therefore, in order to asses for fracture, it is important to know the maximum principal stress. The maximum principal stress distribution on the package after the cool down from the die attach process and the effect of the thermal loading are presented on **Fig. 6** and **Fig. 7**.

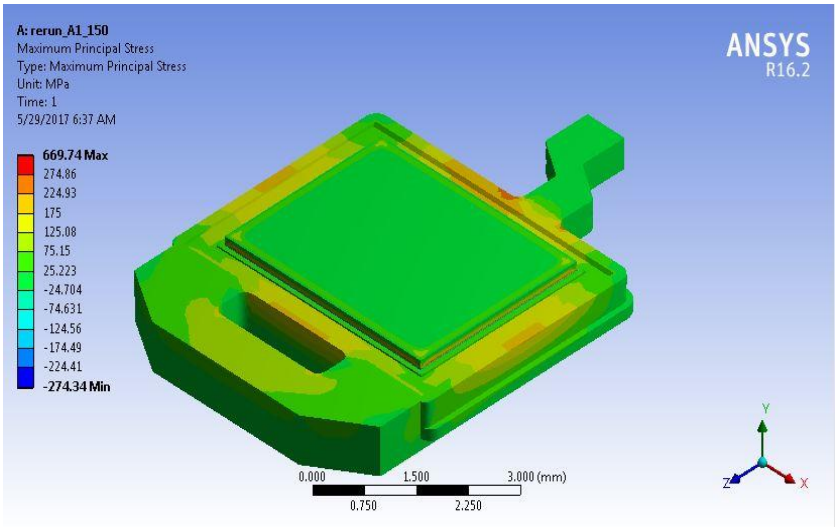

Fig. 6: Maximum principal stress on the whole package

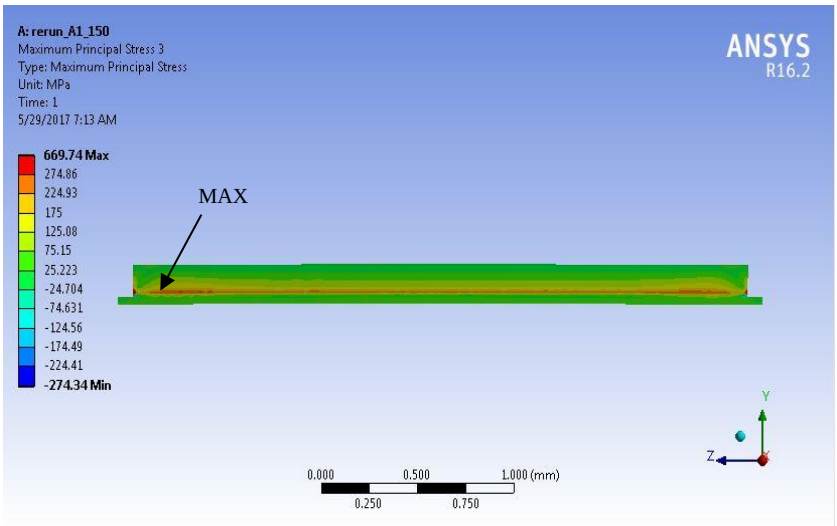

Fig. 7: Maximum principal stress on the die and solder

It can be observed that compared to the other parts of the package, the side surfaces of the die as well as the top surface of the leadframe experience relatively higher stress. Looking closely at the die-solder interface in **Fig. 7**, the maximum principal stress occurs on the silicon die surface near the solder. Stress on the side edges of the silicon die, near its corners and solder interface, was observed to be higher than the stress distribution of the rest of the package. Checking for cracking possibility on these corners and side surfaces was therefore necessary.

In this study, three die size variations and two die thickness variations were done. High stresses were observed in the silicon die-die attach interface. Thus, it is important to investigate how the varying silicon die parameters and changing die attach material affect the maximum

principal stress. Shown in **Fig. 8** is a graph of the Maximum Principal Stress with respect to the die thickness based on Assembly 1 die size. **Fig.** 9 shows the graph of Maximum Principal Stress with respect to the die size, measured in terms of their distances from the neutral axis and at 200µm thickness. Assembly 1 is represented by 2.56 mm distance from the neutral axis, followed by Assembly 2 as 2.16mm and lastly Assembly 3 at 1.76mm. It can be observed that assemblies of die attach 2 have lower stress values compared to assemblies of die attach 1.

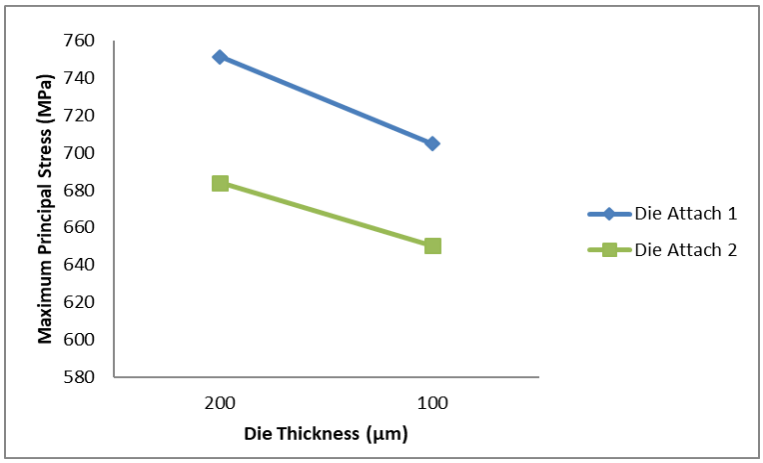

Fig. 8: Maximum principal stress vs die thickness of Assembly 1

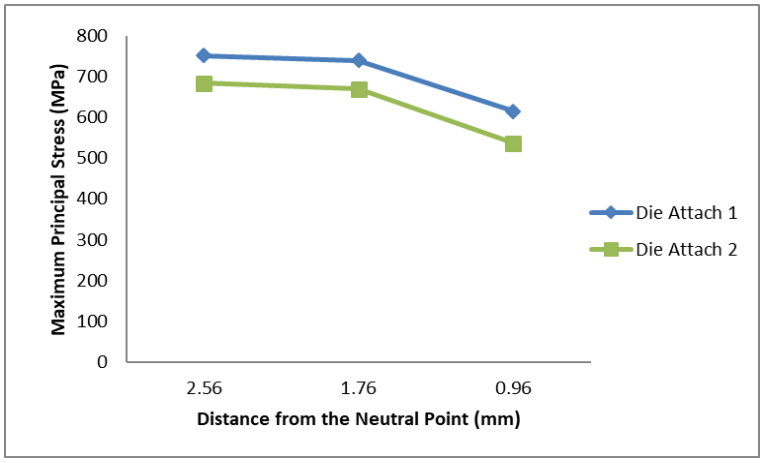

Fig. 9: Maximum principal stress vs distance from the neutral point of Assembly 1

During cooldown from the die attach process, all components undergo certain amount of contractions. The leadframe, compared to the die, contracts significantly greater due to the mismatch of their CTE. This CTE mismatch becomes the primary die stress contributor [2, 17, 18]. How well the die attach binds the leadframe to the silicon die affects the generated stress. Stress is the product of the Young's modulus and strain as shown in **Eqn. 1**. The strain experienced by a material increases as their CTE increases and leads to an equation relating the stress to the Young's modulus and the CTE of a material as shown in **Eqn. 2** [20]. From the material data shown in **Table 2**, it can be seen that die attach 2 has lower modulus of elasticity than die attach 1 by 44%. Lower Young's modulus of the die attach 2 absorbs the

CTE mismatch between the leadframe and the die better than die attach 1 resulting to lower die stresses.

$$\sigma = Ee \quad \textbf{Eqn. 1}$$

where σ is the stress, E is the Young's modulus and e is the strain.

$$\sigma = E\alpha \quad \textbf{Eqn. 2}$$

where σ is the stress, E is the Young's modulus and α is the CTE.

3.2 Finite Element Simulation of Die Crack

In the previous section where the maximum principal stress was computed, the model was assumed to be based on perfect materials without any flaw or defect. This is not the case, however, in reality. Flaws, surface defects and cracks caused by silicon die preparation are present in materials used in the package. Maximum principal stress analysis, however, does not usually consider defects.

In this study, the stresses were found to be concentrated around the corner of the silicon die near the solder as seen on **Fig. 6**. Using the conventional stress analysis, the stresses around the corners of the silicon die will not converge due to the stress singularity and will not be able to obtain the correct solution to the problem. Fracture mechanics-based method was therefore utilized.

The 3μm horizontal crack initiated on the die surface near the die-solder interface was used, which is within the range of the crack length in the studies of Yuning Shi et al. [4] and Calvez et al. [7]. The main objective was to get the J-integral, a fracture parameter, to check if the existing crack can propagate given the thermal conditions the package will undergo. The J-integral values were used to calculate for the stress intensity factor *K*, and were then compared to the fracture toughness K_c of the silicon die.

Given the J-integral obtained from the simulation, *K* of the silicon die can be computed using **Eqn. 3** [14]. Where ν and E are the Poisson's ratio and Young's modulus of the silicon die, respectively.

$$J = G = \frac{K^2(1-\nu^2)}{E} \quad \textbf{Eqn. 3}$$

In this section, the J-integral values obtained in the ANSYS simulation are presented in **Tables 3** and **4** for assemblies with die attach 1 and die attach 2, respectively.

Table 3. Values of J-integral and stress intensity factor (*K)* for Die Attach 1

Die Dimensions (mm)	Thickness (μm)	J-integral (mJ/mm^2)	*K* (MPa-mm^{½})
4.0 x 3.2	200	0.001633	0.539757
	100	0.000315	0.237136
2.75 x 2.2	200	0.001966	0.592309
	100	0.000370	0.257028
1.5 x 1.2	200	0.001150	0.452937
	100	0.000247	0.210016

Table 4. Values of J-integral and stress intensity factor (*K)* for Die Attach 2

Die Dimensions (mm)	Thickness (µm)	J-integral (mJ/mm^2)	*K* ($MPa\text{-}mm^{½}$)
4.0 x 3.2	200	0.000442	0.280902
	100	0.000355	0.251502
2.75 x 2.2	200	0.000535	0.308893
	100	0.000315	0.237015
1.5 x 1.2	200	0.000580	0.321570
	100	0.000437	0.279354

The computed *K* from the simulations were below the monocrystalline silicon's critical fracture toughness of 0.83-0.95 $MPa\text{-}mm^{1/2}$ [19], as seen on **Tables 3** and **4**. This indicates that in all the geometric variations, the crack will not likely propagate at the given conditions. It is noteworthy, however, that the calculated stress intensity factor for the 200 µm thick die for all the die sizes can still be considered near critical since it is almost 60% of K_c in the ideal condition. If other defects are present in the die, *K* could increase and the possibility of crack growth also increases. It is also equally important to look at the trends of the J-integral as the die size and die thickness decrease. Plots of the J-integral with respect to the die thickness and the die sizes are shown in **Figs. 10** to **13**.

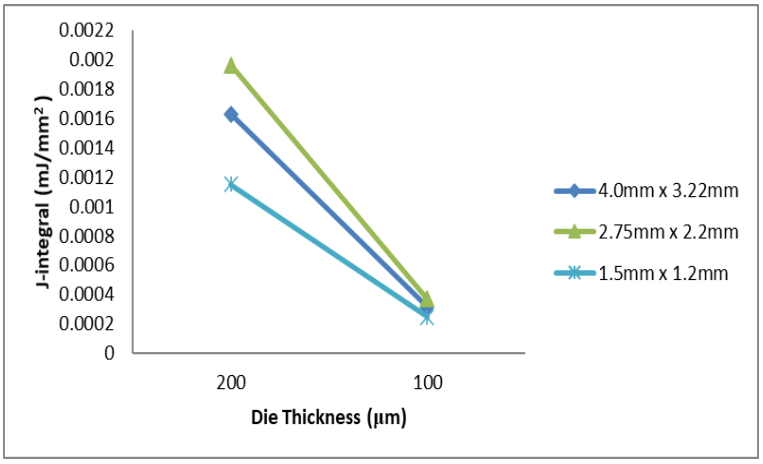

Fig. 10: J-integral vs die thickness with die attach 1

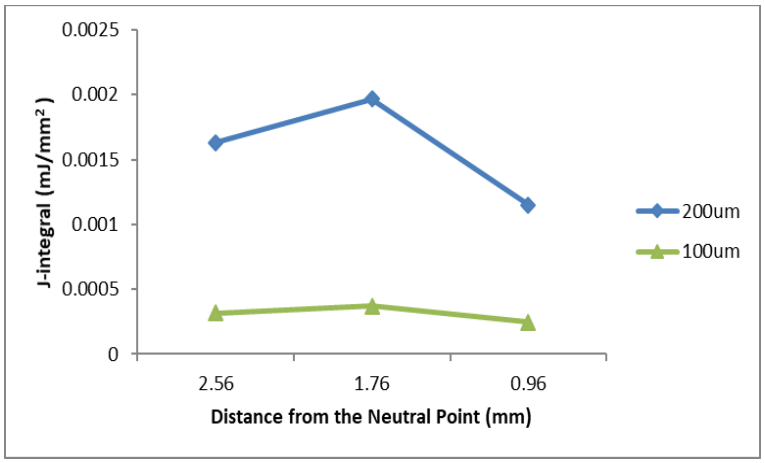

Fig. 11: J-integral vs die size for die attach 1

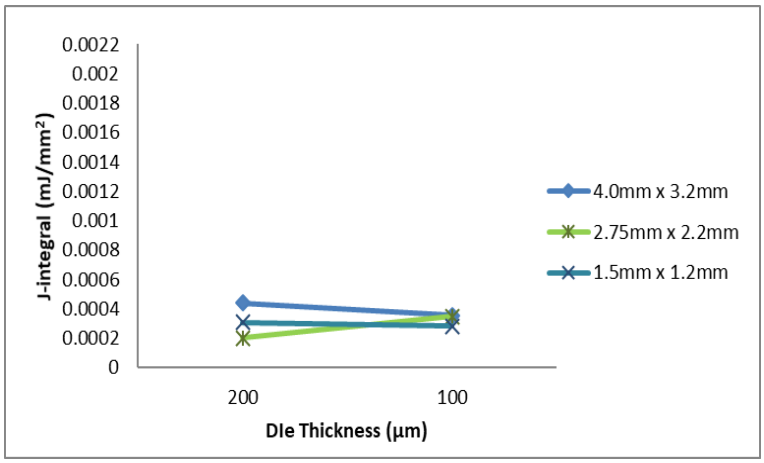

Fig. 12: J-integral vs die thickness for die attach 2

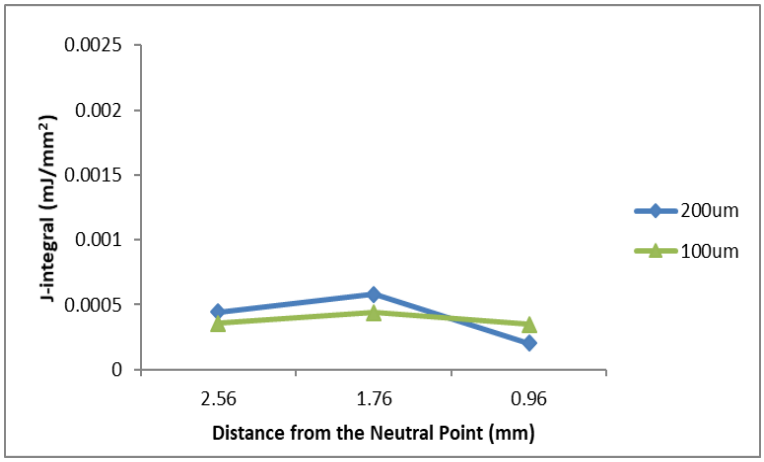

Fig. 13: J-integral vs die size for die attach 2

Fig. 10 and **Fig. 12** show that the thickness of the die greatly affects the behavior of the crack. The risk of crack propagation is exhibited by the value of J-integral where the increase in its value also increases the risk of crack propagation. It is also observed that the J-integral is generally high at the 200μm thickness, and low at 100μm.

The primary driving force in die crack is the CTE mismatch between the die and leadframe which is affected by how well these two materials are bound by the die attach material. Die crack is also affected by how much the die or the leadframe opposes the relative contraction and expansion during the thermal loadings they are subjected to. A more rigid die will oppose the relative contraction more than a compliant one. Hence, the trend was that J-integral decreases with the die thickness decreases. This trend was found to be similar to Chong's study [3], wherein they tested different thicknesses of silicon die for their strength using a three point bending test. Their tests show that thicker silicon die will most likely fail earlier compared to thinner die. Thicker die, which is more rigid, cannot absorb higher stresses as good as thinner die. Thinner die, due to its flexibility, can absorb higher stresses before failing.

The graph relating the J-integral to the die size is presented on **Fig. 11** and **Fig. 13**. It was observed from the plot that die size does not have significant influence on the J-integral as compared to the effect of the die thickness. It shows that die size only affects the thick die, while on thin die, there seems to be no effect. In the 200μm thick die, it can be seen that the value of the J-integral slightly decreases as the distance from the neutral point decreases or as the die size becomes smaller. However, the die size effect is not evident with a die thickness of 100μm.

IV. CONCLUSION

The simulations show that in the die attach cooling process, high stress distribution occurs at the die surfaces near the die attach material. The maximum principal stress was located at one of the corners of the die at the die-solder interface. It was therefore necessary to check on that location for die cracking. It is also observed that the maximum principal stress was observed to decrease with the die thickness. This was mainly attributed to the CTE mismatch of the components. The higher the modulus of elasticity of the die attach material, the higher the thermal stress it experiences.

Considering the horizontal crack on the silicon die, the J-integral was used to evaluate the risk of crack propagation of a 3μm crack. It was concluded that the optimum die thickness was at 100μm for both die attach materials. It can also be said that for die attach 2, which has lower modulus of elasticity, has lower risk of crack propagation, as seen on their stress intensity factor K.

Different geometric and material parameters have varying effects on the risk of crack propagation. The J-integral values obtained in all simulations show that the initiated crack on the die is not likely to progress. The trend on how the crack behaves as different geometric and material properties is changed; however, it is still essential in predicting when the crack might propagate.

The behavior of the crack or the trends in the stresses obtained in this study shows that reduction in die size is not expected to greatly affect die cracking. Whereas, a reduction in die thickness is generally expected to reduce die crack risk. Therefore, it can be inferred from the study that continuous miniaturization can still be done but with careful consideration on the limits of the die thickness especially for die attach material with high modulus of elasticity.

NOMENCLATURE

CTE	coefficient of thermal expansion (1E-6/K)	K_c	critical stress intensity factor (MPa-mm$^{1/2}$)
E	Young's modulus (GPa)	SOD	small outline diode
G or J	energy release rate (mJ/mm^2)	SOT	small outline transistors
K	stress intensity factor (MPa-mm$^{1/2}$)	ν	Poisson's ratio

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