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A DESIGN METHODOLOGY FOR IMPLEMENTING RF CMOS LOW-NOISE AMPLIFIERS IN A 0.25 μM CMOS PROCESS

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ABSTRACT

In this paper, a methodology in designing CMOS Low-Noise Amplifiers (LNAs) in a 0.25-μm CMOS process is proposed. Three power-matching techniques are considered in the design of the LNA. These are: (1) matching for maximum available gain, (2) matching for a constant gain, and (3) matching for stability. Twenty-two LNA circuits employing the common-source topology with cascode configuration are designed, implemented, fabricated, and tested. These circuits differ from each other in terms of the transistor dimensions, inductor and capacitor implementations, and bias voltages used. The performance of LNA circuits designed using the three different techniques are characterized. Simulation and actual measurement results are also compared and analyzed to determine the capability of the simulator to predict the LNA's overall performance at radio frequencies.

I. INTRODUCTION

Wireless technology continues to evolve at a very rapid pace. The sudden growth in the number of mobile phone subscribers globally is a strong evidence of this trend. This growth provides challenging opportunities for research and development. Today's consumers, for example, want portable handsets that are not only compact and affordable, but also offer additional features possible with the latest technology. The strong demand for portable wireless communication systems motivates the research of low cost, low power and high performance devices. Single-chip integration of transceivers with RF front-end and digital processor is seen to be a possible solution to these particular requirements.

As the feature size of Complementary Metal Oxide Semiconductor (CMOS) technology continues to decrease, cutoff frequency of the transistor improves which makes it highly suitable for RF applications [1]. Aside from this, CMOS technology is inherently low cost and compatible with mixed signal applications. It also has high integration density, low voltage capability, and production maturity. Hence, the use of CMOS is very attractive for integrating digital and RF modules in a single chip.

II. RF CMOS Low-Noise Amplifiers

Low noise amplifiers (LNAs) represent one of the basic building blocks of a communications system. Typically, as illustrated in Figure 1, it is part of the first stage of a radio receiver [2]. In real-world situations, such as cellular phone systems, the received signal is very low in power and must be amplified before the information it contains can be properly demodulated. However, all amplifiers add noise to the signals that they boost and when amplifying a very low-level signal, as in the case of an LNA, the amplifier's own noise can actually swamp the signal [3].

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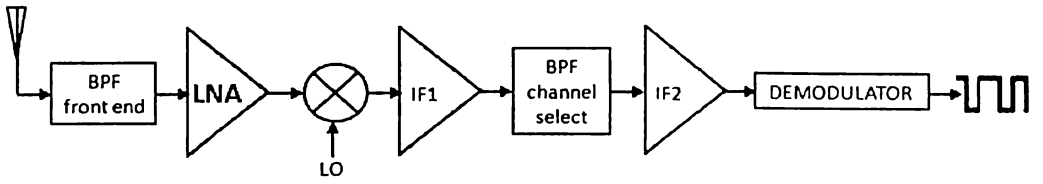


Figure 1. Block diagram of a typical receiver [4]

LNA design involves a number of tradeoffs among several figures of merit, such as the gain, noise, power, impedance matching, stability, and linearity [5]. These multi-dimensional tradeoffs define common goals in LNA design. These include minimizing the noise figure of the amplifier, providing gain with sufficient linearity, and providing a stable 50 Ω input impedance to terminate an unknown length of transmission line [1].

2.1 LNA Topology

The most commonly used topology in CMOS LNA design is the common source topology with cascode configuration. The schematic diagram of this topology is shown in Figure 2. The cascode configuration is composed of a common source transistor (M_2) stacked with a common gate transistor (M_1). Cascoding of MOSFETs has become a standard in the design of CMOS LNAs [6]. This is the topology of choice for high-frequency applications because transistor M_1 reduces the Miller effect by decreasing the input transistor's gate-to-drain capacitance; hence, the cascode configuration keeps the Miller effect from degrading the power gain and increasing the input-referred noise. Aside from this, the cascode configuration also improves reverse isolation, increases stability, and reduces interaction between the tuned input and tuned output in an LNA [1], [7].

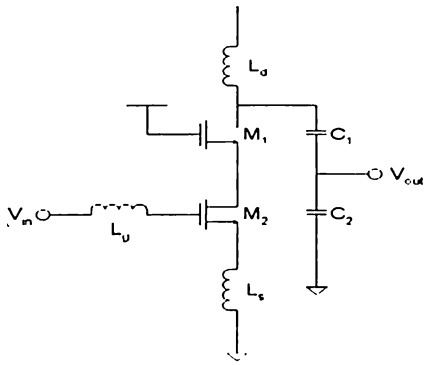


Figure 2. Common source with cascode configuration

Due to the many advantages that this topology offers, this topology is used in the design of LNA circuits implemented. To aid in the design of the circuit, the input and output impedance matching networks are discussed next.

Input Impedance Match

Assuming that the input and output of the LNA are effectively isolated, i.e. $|S_{12}|$ is greater than 30 dB, the input impedance of the circuit may be derived from the small-signal equivalent circuit of the common-source topology presented in Figure 3.

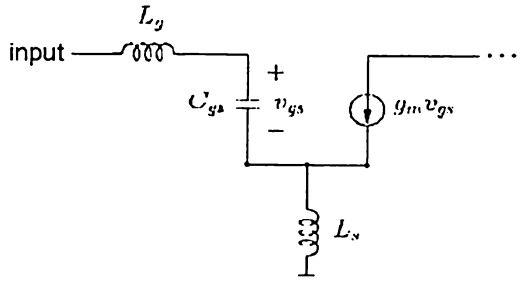


Figure 3. Small-signal equivalent circuit of the LNA's input.

Solving for the input impedance gives:

$$Z_{in} = j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \tag{1}$$

At resonance, the inductive and capacitive components of the input cancel each other, i.e. the imaginary part of the input impedance is zero. Thus, the resonant frequency, ω_o, can be derived from equation 1 by equating the sum of the imaginary part to zero and solving for ω.

$$\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \tag{2}$$

As such, the impedance is purely real at the resonant frequency and is given by:

$$Z_{in} = \omega_T L_s \tag{3}$$

where

$$\omega_T = \frac{g_m}{C_{gs}} \tag{4}$$

According to equation 3, the impedance is purely real and proportional to the source inductance, L_s, at the resonant frequency. Hence, this topology is suitable for narrowband applications only. The desired 50 Ω impedance can be achieved with proper choice of L_s. Once the value of the source inductance is determined, the gate inductance, L_g, value can be calculated to set the resonant frequency using equation 2 [8].

Output Impedance Match

In order to interface the LNA with the test equipment, the output of the LNA in Figure 2 must be converted to 50Ω. To accomplish this, the capacitive divider [9] shown in Figure 4 is used.

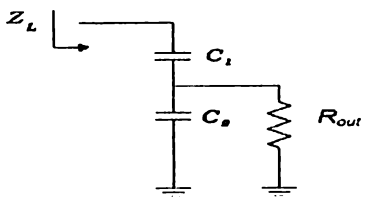


Figure 4. Capacitive divider as impedance transformer.

The real part of the impedance Z_L is now equal to:

$$real(Z_L) = \frac{1+[\omega_o R_{out}(C_1+C_2)]^2}{\omega_o{}^2 R_{out} C_1{}^2} \tag{5}$$

and the equivalent capacitance that the capacitive divider presents to the output of the LNA is

$$C_{eq} = \frac{C_1+\omega_o{}^2 R_{out}{}^2 C_1(C_1+C_2)C_2}{1+[\omega_o R_{out}(C_1+C_2)]^2} \tag{6}$$

If $[\omega_o R_{out}(C_1+C_2)]^2 >> 1$ then equations 5 and 6 simplify to

$$real\ (Z_L) \approx R_{out}\left[1+\frac{C_2}{C_1}\right]^2 \tag{7}$$

$$C_{eq} \approx \frac{C_1 C_2}{C_1+C_2} \tag{8}$$

The capacitive impedance matching network must transform the real part of Z_L to the output resistance, R_{out}, which is equal to 50 Ω. To have a clearer picture on the dependencies of the output resistance, equation 7 is manipulated algebraically to give:

$$R_{out} \approx \frac{real\,(Z_L)}{\left[1+\frac{C_2}{C_1}\right]^2} \tag{9}$$

This shows that the output resistance is proportional to the output impedance seen at the drain of M2. Moreover, the output resistance is inversely proportional to the C_2/C_1 ratio.

The output inductor, L_d, in Figure 2 is designed to resonate at ω_o with the node capacitance at the drain of M_1. The effective capacitance seen at the drain of M_1 is a parallel combination of the equivalent capacitance, C_{eq}, introduced by the capacitive divider network, the drain-to-gate capacitance, C_{dg}, the drain-to-bulk capacitance, C_{db}, and the parasitic shunt capacitance of the drain inductor. Representing the last three capacitances by a lumped capacitor C_{out}, L_d is derived from the following equation:

$$\omega_o = \frac{1}{\sqrt{L_d(C_{out}+C_{eq})}} = \frac{1}{\sqrt{L_d\left(C_{out}+\frac{C_1C_2}{C_1+C_2}\right)}} \quad (10)$$

The above equation illustrates the inverse dependence of the resonant frequency on the values of L_d, C_1, C_2, and the effective output capacitance seen at the drain of M_1.

Note that the input and output tank can be designed to resonate at the same frequency to provide a narrow-band gain, but can also be made to offset each other to provide a broader and flatter frequency response [10].

2.2 Power Matching Tehniques

In RF circuit design, power matching is synonymous to impedance matching. Maximum power transfer between two circuits is achieved when the impedances of the two circuits are matched. There are three commonly-used techniques in power matching. The first one shows how to match an LNA in the maximum available gain condition. The second deals with an LNA matched for a desired constant gain. Lastly, the third technique involves matching for circuit stability.

Matching for Maximum Available Gain (MAG)

For a nonzero S_{12} parameter, maximum available gain is achieved under simultaneous conjugate matching conditions. This means that the output match affects the input match and vice-versa. Correspondingly, maximum available gain is the highest gain that can be expected from a two-port network under conjugately matched conditions [11]. In order to obtain maximum gain conditions, the source reflection coefficient must be equal to the conjugate of the input reflection coefficient.

$$\Gamma_S = \Gamma_{in}^* \quad (11)$$

Similarly, the load reflection coefficient must be the same as the conjugate of the output reflection coefficient.

$$\Gamma_L = \Gamma_{out}^* \quad (12)$$

Before starting with any design calculation, stability must first be checked using the Linvill stability factor, K [11].

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta S|^2}{2|S_{21}S_{12}|} \quad (13)$$

Once unconditional stability is realized, the maximum available gain, expressed in dB, is computed from the S-parameter using the following equation [11].

$$MAG = 10\log\frac{|S_{21}|}{|S_{12}|} + 10\log(K-\sqrt{K^2-1}) \quad (14)$$

The next step would be to find the load reflection coefficient needed for a conjugate match [11]:

$$\Gamma_L = \frac{B_2 \pm 2|S_{12}S_{21}|\sqrt{K^2-1}}{2C_2} \quad (15)$$

where [11]

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta S|^2 \quad (16)$$

$$C_2 = S_{22} - S_{11}^{*}\Delta S \quad (17)$$

Note that in equation 15, if B_2 is positive, then the – sign must be used before the term with the radical. Correspondingly, for a negative B_2, the + sign is used.

After the value of the load reflection coefficient is derived, the corresponding source reflection coefficient can be computed using the proceeding equation.

$$\Gamma_S = \frac{B_1 \pm 2|S_{12}S_{21}|\sqrt{K^2 - 1}}{2C_1} \quad (18)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta S|^2 \quad (19)$$

$$C_1 = S_{11} - S_{22}^{*}\Delta S \quad (20)$$

Once the source and load reflection coefficients are known, the input and output matching networks can be designed with the aid of the Smith chart.

Matching for a Constant Gain

An LNA should be simultaneously conjugately matched to its source and load only if maximum gain is desired, and without regard for other parameters such as noise figure and bandwidth. A controlled and manageable way to limit gain by not matching the LNA to its load is called *selective mismatching*.

One of the easiest methods for selectively mismatching an LNA is by using a constant-gain circle plotted on a Smith chart [11]. The equations for obtaining the center and radius of the circle are given by:

$$Center = \frac{(S_{22}^{*} - \Delta S^{*} S_{11})G}{(1 + G(|S_{22}|^2 - |\Delta S|^2))} \quad (21)$$

$$Radius = \frac{\sqrt{1 - 2K|S_{12}S_{21}|G + |S_{12}S_{21}|^2 G^2}}{(1 + G(|S_{22}|^2 - |\Delta S|^2))} \quad (22)$$

where

$$G = \frac{(G_{DESIRED})}{|S_{21}|^2} \quad (23)$$

$$C_2 = (S_{22} - \Delta S S_{11}^{*}) \quad (24)$$

$$D_2 = |S_{22}|^2 - |\Delta S|^2 \quad (25)$$

The desired gain, $G_{DESIRED}$, is set by design specifications. It should be stressed that the *MAG* limits the gain. Thus, the *MAG* must be computed using equation 14 to have insight on the feasible gain levels that can be achieved.

The load reflection coefficient from any point in the constant-gain circle can then selected provided that stability is satisfied. Once the load reflection coefficient is known, the source reflection coefficient can be calculated. This would then lead to the determination of the necessary input and output matching networks.

Matching for Stability

When the S-parameters obtained from inductively-generated cascode amplifier do not meet the stability requirement ($K>1$), *matching for stability* must be used in the design of the matching networks.

In this technique, output stability circles are drawn. The center and radius equations are given by:

$$Center = \frac{S_{22}^{*} - S_{11}\Delta S^{*}}{|S_{22}|^{2} - |\Delta S|^{2}} \tag{26}$$

$$Radius = \frac{|S_{12}S_{21}|}{|S_{22}|^{2} - |\Delta S|^{2}} \tag{27}$$

The load reflection coefficient that would provide the desired gain is then chosen in the stable areas of the Smith chart as dictated by the stability circles. Similar to the previous technique, the source reflection coefficient can then be obtained, and the matching networks established.

If the locus of points representing the desired gain does not fall on stable areas of the Smith chart, then a compromise on the desired gain must be done to insure circuit stability.

III. Design Methodology

The first step in the design of LNAs is to determine the transistor sizes to be used. Initial experiments done in the laboratory [12] showed that transistor widths ranging from 250-350 μm for minimum channel length transistors are adequate for this study. It is also worth mentioning that it is useful and desirable to use the minimum length cutoff frequency, f_t [9] and decrease the minimum noise figure [2].

Once the transistor width is selected, the circuit is simulated to get the initial S-parameters of the design. The *n2port* component, which is a component of the simulator that accepts S-parameter data as input, is used to represent the source inductor. In this study, all spiral inductors used were simulated in ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits) [13]. Hence, the need for *n2port* components in the simulation of the whole LNA circuit is inevitable. ASITIC is a tool that uses electromagnetic simulation to analyze spiral inductors.

The input voltage is then adjusted such that the circuit is stable, i.e. $K > 1$ and $|\Delta S| < 1$, at the desired resonant frequency. Upon the determination of a stable input bias, the source and load reflection coefficients are computed. Subsequently, the source and load impedances are calculated using the following equations:

$$Z_S = \frac{1+\Gamma_S}{1-\Gamma_S} \tag{28}$$

$$Z_L = \frac{1+\Gamma_L}{1-\Gamma_L} \tag{29}$$

The matching networks are then designed with the aid of a Smith chart. Note that in order to maintain the circuit topology in Figure 2, the input matching network must be composed of a series inductor (L_g) and the output matching network must be a pi-network consisting of a shunt capacitor (C_p), a series capacitor (C_l), and a shunt inductor (L_d). This is illustrated in Figure 5.

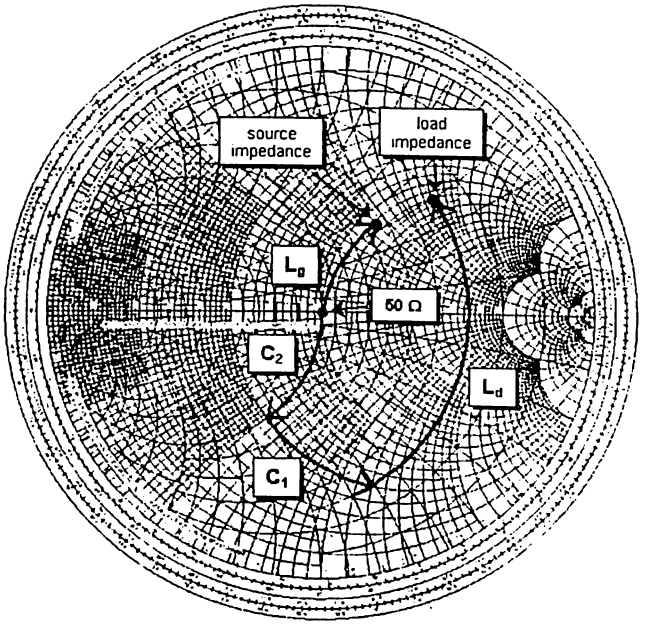


Figure 5. Smith chart showing the transformation of the input and output impedances to 50 Ω.

The corresponding inductor and capacitor values are then computed based on the amount of impedance represented by the distances covered in the Smith chart. After computation of the component values, the complete circuit is again simulated, with the transistors' parasitics extracted from the layout.

If the resonant frequency shifts due to the effects of the MOSFET parasitics, tuning of the circuit is executed by adjusting the values of L_g and/or L_s. Once the circuit is tuned to the desired frequency, the gain is determined depending on which power matching technique is used. If the circuit gain, which is the magnitude of S_{21}, is not comparable to the desired gain, the input voltage is increased until comparable values are obtained in the computation and simulation.

Thereafter, the layout of the capacitors and the routing wires are incorporated into the circuit simulation. The degradation in the circuit's performance is then recorded via the new set of S-parameters.

IV. Results and Analysis

To aid in the analysis of results, a small-signal equivalent circuit of the LNA, shown in Figure 6, is developed. The input transistor (M_2) model is fashioned after the basic small-signal model of the transistor, which is composed of the gate-to-source capacitance, *Cgs*, and the voltage-controlled current source. The cascode transistor *M1* is denoted by the resistor $gmro^2$, which is the output resistance of the cascode amplifier. The passive devices comprising the matching networks are also incorporated in this circuit. The input and output impedances (*Zin* and *Zout*) are included to accurately predict the LNA's behavior. *Zin* and *Zout* are calculated by first converting the measured LNA S-parameters to Z-parameters and using the relationships $Z_{in} = Z_{11}$ and $Z_{out} = Z_{22}$.

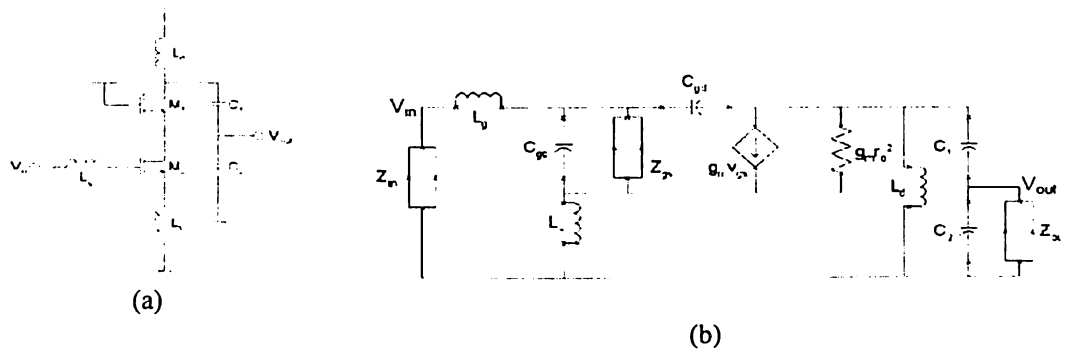


Figure 6. (a) LNA schematic circuit and (b) its small-signal equivalent circuit.

The impedance *Zgs* is a lumped representation of the gate resistance of transistor *M2* and other parasitic resistances and reactances present in the circuit. The gate resistance plays a very significant role in the performance of the transistor at RF [14, 15]. The parasitics of other components of the LNA are also included with *Zgs*. This equivalent circuit model is used to analyze results obtained from on-wafer measurements.

Figures 7 and 8 illustrate the difference between the simulation results and the results obtained from the on-wafer testing of the reference circuit. These figures generalize the following results obtained for all the circuits:

(1) actual S_{11} peak frequency is higher than what is obtained in the simulations,
(2) better input matching, i.e. larger $|S_{11}|$, is observed in the actual measurements,
(3) actual tests show an improvement in the LNA's isolation,
(4) lower gain is achieved in the actual testing of the circuit,
(5) actual S_{21} peak frequency is comparable to the simulated S_{21} peak frequency,
(7) actual S_{22} peak frequency is less than what is obtained in the simulations,
(8) poorer output matching characteristics is observed in the actual testing results, and
(9) actual testing results show improvement in stability.

These discrepancies between the simulated and actual measurement results clearly indicate that the simulator was not able to accurately predict the behavior of the circuit. Some factors that may have contributed to these discrepancies are discussed in the succeeding paragraphs.

Input Match

The SPECTRE simulator employs the BSIM3v3 model of the transistor, and thus does not take into account the transistor's gate resistance. At RF, the gate resistance dominates the input reflection coefficient of the transistor [16]. This gate resistance is depicted as R_g in the small-signal circuit shown in Figure 9. Modifying equation 3 to include the gate resistance gives:

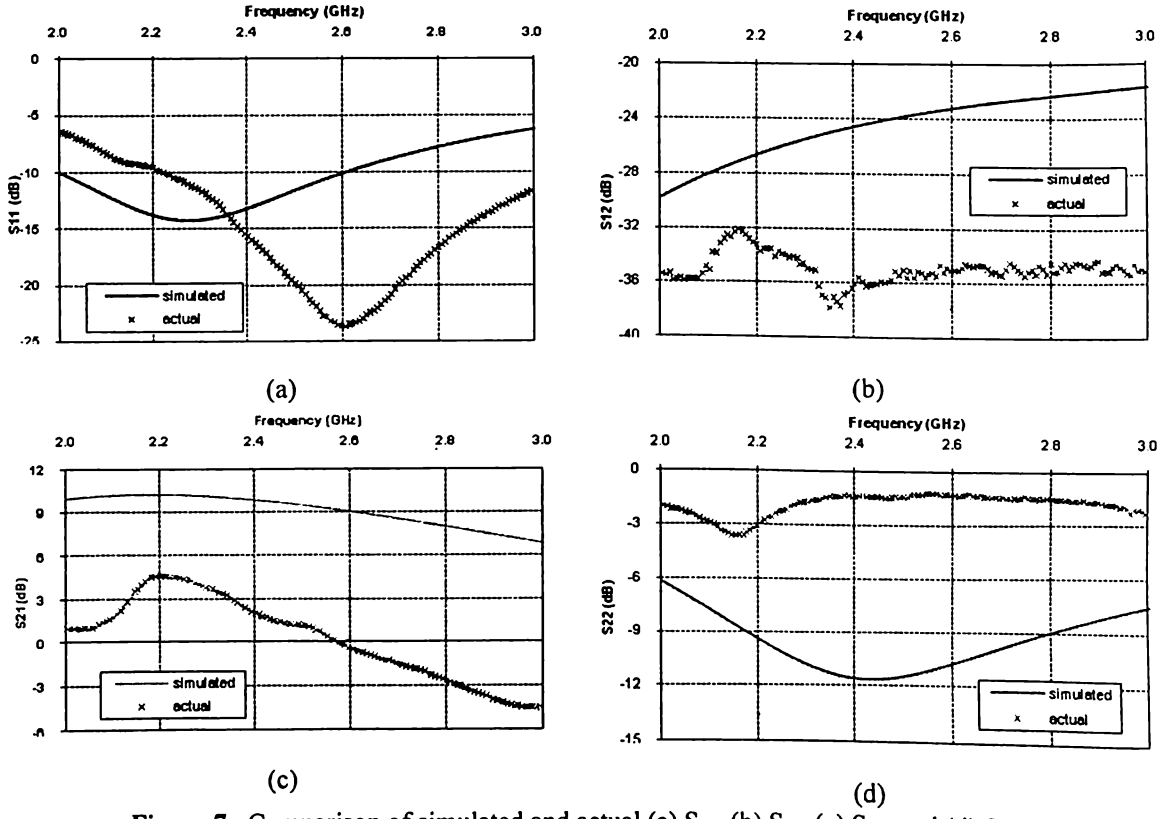


Figure 7. Comparison of simulated and actual (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22} of LNA circuit. $V_{DD} = V_{CASC} = 2.5$ V. Supply current maintained at 4.1 mA.

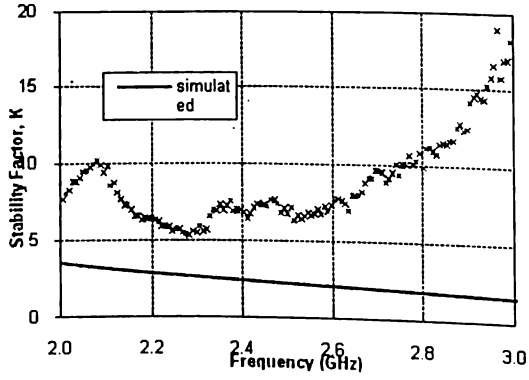


Figure 8. Comparison of simulated and actual extracted stability factor of reference LNA circuit for $V_{dd}=V_{casc}=2.5$V. Supply current maintained at 4.1 mA.

$$Z_{in} = R_g + \left(\frac{g_m}{C_{gs}}\right)L_s \tag{30}$$

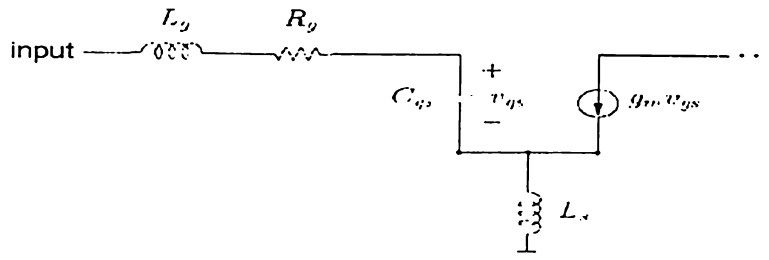


Figure 9. Small-signal equivalent circuit of the input matching network including the gate resistance.

Thus, the lack of gate resistance in the SPECTRE transistor model is one factor that contributes to the difference in $|S_{11}|$ between the simulated and actual measured results. In fact, the effective input resistance in the simulations is lower than 50 Ω while actual measurement results show effective input impedance to be larger than 50 Ω. Figure 10a shows the comparison among the effective input resistances of actual, simulated with no gate resistance and simulated with gate resistance of the reference LNA circuit. As can be observed from the figure, the effective input resistance of the actual measurement deviates from the simulations by around 30-40 Ω. This range of values is consistent with the values of extracted RF MOSFET gate resistances in a study by Gutierrez [17] for the same CMOS process. This was also verified when extracting the value of Z_{gs} in Figure 6b from on-wafer measurements.

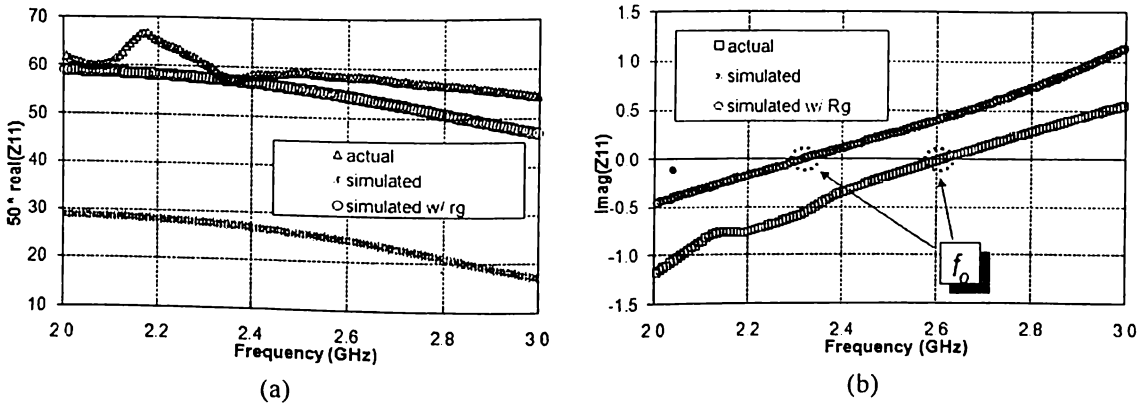


Figure 10. (a) Real and (b) imaginary part of Z_{11} of the reference LNA circuit. $V_{DD} = V_{CASC} = 2.5$ V. Supply current maintained at 4.1 mA.

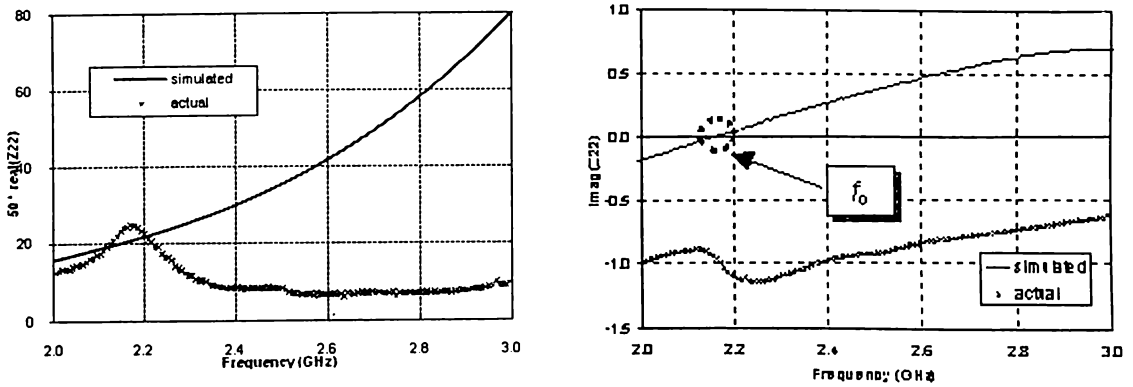
The resonant frequency, f_o, at the input is the frequency at which the capacitive and inductive reactances cancel each other out. In Figure 10b, it can be observed that the actual resonant frequency is higher than the simulated resonant frequency at the input. It can also be observed that the gate resistance has no significant effect on the resonant frequency at the input. Looking at Figure 7a, it can be deduced that the peak frequency of the input is the same as its resonant frequency. As can be inferred from equation 31, the resonant frequency of the input is inversely proportional to the sum of the source and gate inductors, and the gate-to-source capacitance of the transistor. In [18], it was observed that ASITIC simulation of spiral inductors closely predicts the actual inductance value for frequencies less than 4 GHz. Therefore, the deviation in the resonant frequency of the input is attributed to the simulator's extraction of the

MOSFET gate-to-source capacitance. From the results obtained, it can be concluded that the simulator over-estimates the gate-to-source capacitance of the transistor; hence, the simulated resonant frequency is lower.

$$\omega_o = \frac{1}{\sqrt{C_{gs}(L_s + L_g)}} \tag{31}$$

Output Match

Referring back to Figure 7d, it can be observed that the magnitude of S_{22} is smaller in the actual measurements as compared to the simulations. Figure 11 illustrates a comparison between the simulated and actual effective output impedance, Z_{22}.



(a) (b)

Figure 11. (a) Real and (b) imaginary part of Z_{22} of the reference LNA circuit. $V_{DD} = V_{CASC} = 2.5$ V. Supply current maintained at 4.1 mA.

The difference in the effective output impedance between the simulations and actual measurements can be explained by the equation for the output resistance, R_{out}, in equation 9. This states that R_{out} is dependent on Z_L, which is the impedance seen at the drain of M_1, and on the ratio of C_2 to C_1. Tan [19] determined that the actual capacitance of VPP capacitors within the range of values used for C_1 and C_2 in this research is around 4% - 5% larger than the extracted capacitance of the simulator. Since equation 9 involves a ratio of two capacitors with actual values that deviates from the simulations by almost the same amount, then the significant change in the effective output impedance of the LNA cannot be attributed to the capacitive divider network. Therefore, the difference between the simulated and actual measurement results is due to the impedance Z_L. This is verified by a research done by Cabuling et al. [20], which includes the characterization of the DC behavior of an NMOS transistor for the same CMOS process as the one used in this study. Figure 12 shows the I_d *vs.* V_{ds} curve for an NMOS transistor with an aspect ratio of 200/0.8. Note that the output resistance of the transistor is given by:

$$\frac{1}{r_o} = \frac{dI_d}{dV_{ds}} \tag{32}$$

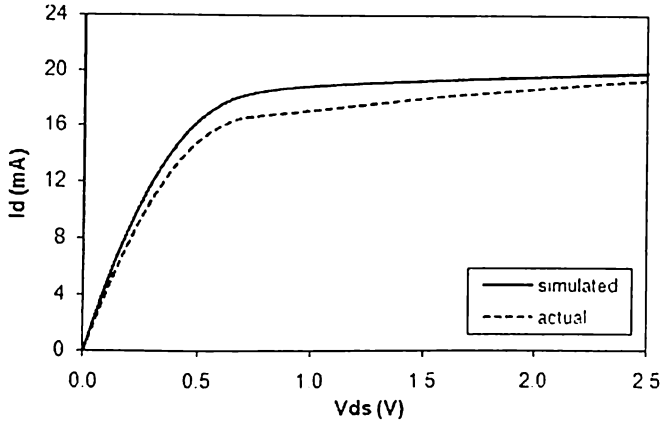


Figure 12. DC behavior of NMOS transistor (W = 200 μm, L = 0.8 μm). [20]

Looking at Figure 12, the slope of the actual DC curve is steeper compared to the simulated curve. This means that the actual results show a larger slope. Since the output resistance is the inverse of the slope, then the actual output resistance is smaller than the simulated output resistance. In fact, when the output resistance of the two curves at V_{ds} = 2.5 V is computed, the output resistance is determined to be equal to 1.67 kΩ and 123 Ω for the simulated and actual DC curves, respectively.

In Figure 11b, it can be observed from the actual results that the circuit did not resonate since it did not cross the y-axis. A negative value for the imaginary part of Z_{22} means that the reactance seen at the output node is capacitive. The actual results exhibit a capacitive reactance from 2-3 GHz while in the simulations, the reactance starts to become inductive near 2.2 GHz. One reason for this is the fact that the pad parasitics were not completely eliminated after de-embedding.

Another factor that caused the significant difference between the simulated and actual S_{22} is the lack of a substrate network in the BSIM3v3 transistor model. A substrate network model is shown in Figure 13 and shows the relationship of the substrate admittance, Y_{sub}, to the components of the substrate network. Jen et al. [21] demonstrated that the effective admittance of the substrate network could reach up to 50% of the total output admittance. The substrate coupling effects play an important role for the output reflection coefficient through the drain and source junctions of a transistor and the substrate resistances [16], [21], [22]. The substrate resistance is responsible for the roll-off of the output resistance at RF [23]. This decrease in the output resistance is verified in Figure 11a where a considerable reduction in the actual resistance is observed. Also, at high frequencies, the signal at the drain couples to the source and bulk terminals through the junction capacitance, C_{jdb}, and the substrate resistance, R_{sub}, [24]. This capacitive coupling effect contributes to the deviation between the simulated and actual measurement results [17].

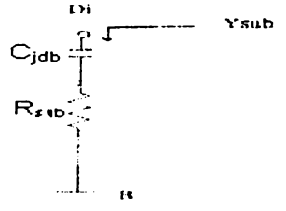


Figure 13. Simplified equivalent circuit of the substrate network. [22]

$$Y_{sub} = R_{sub}(\omega C_{jdb})^2 + j\omega C_{jdb} \quad (33)$$

Gain and Isolation

The decrease in the gain (S_{21}) shown in Figure 14a is the result of the poor output match observed during the on-wafer testing of the circuits. On the other hand, the improvement in isolation (S_{12}) shown in Figure 14b is caused by the decrease in the signal power of the transmitted wave at the input port of the LNA. This decrease is due to the better input matching characteristics of the actual circuit. The observed improvement in isolation also suggests that the actual circuit has a larger input to output impedance than what the simulation results predict.

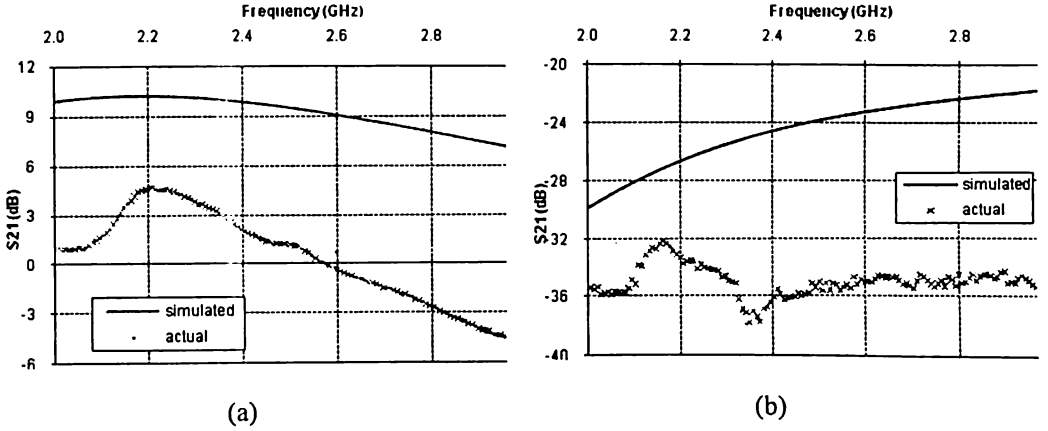


Figure 14. Comparison of simulated and actual (a) gain and (b) isolation of the reference LNA circuit. $V_{DD} = V_{CASC} = 2.5$ V. Supply current maintained at 4.1 mA.

Power Matching Techniques

Three power matching techniques were investigated in this paper. As expected, the circuit employing the *MAG* technique has the highest gain and the circuit employing the *stability* technique was the most stable of the three. These trends are shown in Figure 15. Hence, the choice of the technique to be implemented would depend on whether the gain or stability is more important for the intended application of the LNA. For a compromise between the gain and stability characteristics of the LNA, the *CG* technique may be employed.

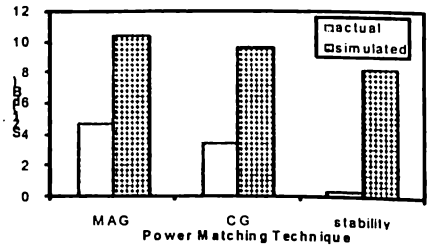


Figure 15. LNA gain for different power matching techniques.

V. Conclusions

In this paper, 22 LNA circuits employing the common-source topology with cascode configuration were designed and fabricated using a standard 0.25μm CMOS process. A step-by-step design methodology, which utilizes the Smith chart in the design of the matching networks and is adapted from conventional discrete component RF circuit design, was used. These LNA circuits were then characterized in terms of the following parameters: (1) power consumption, (2) peak frequencies, (3) input and output matching characteristics, (4) gain, (5) isolation, and (6) stability.

To aid in the analysis of the measured results, a small-signal equivalent circuit that includes a lumped representation of the effective gate impedance was derived. This equivalent circuit assumes that all other components of the LNA are ideal. Hence, the effect of parasitic resistances and reactances are lumped together in the gate impedance, Z_{gs}.

The fabricated LNA circuits were also tested to characterize difference in performance between simulated and actual simulation results. Large discrepancies between the simulated and actual measurement results were obtained; thus, verifying the inability of the simulator to predict the actual performance of the circuit.

In general, the actual S_{11} peak frequency is greater than the simulated results because of the simulator's over-estimation of the transistor's gate-to-source capacitance. Improvements in the input match of the LNA were also observed through on-wafer measurements. This is due to the lack of the gate resistance in the BSIM3v3 transistor model utilized by the simulator. In contrast, actual measurements showed a decrease in the S_{22} peak frequency and a very significant degradation in the output matching characteristics of the LNA. These discrepancies are due to: (1) the absence of the substrate network in the transistor model used in the simulations, (2) the significantly smaller output resistance of the transistor obtained from actual measurements as compared to simulations, and (3) the inaccurate extraction of parasitic capacitances and resistances by the simulator. Because of the poor output match obtained in the on-wafer measurements, lower gains were achieved. This led to improvements in the circuit's stability and isolation property.

Three power matching techniques were also investigated in this paper. These are *matching for maximum available gain (MAG)*, *matching for a constant gain (CG)*, and *matching for stability*. As expected, the circuit employing the *MAG* technique has the highest gain and the circuit employing the *stability* technique was the most stable of the three. Hence, the choice of the technique to be implemented would depend on whether the gain or stability is more important for the intended application of the LNA. For a compromise between the gain and stability characteristics of the LNA, the *CG* technique may be employed. Note that the choice on the technique to be used must be done at the beginning of the LNA design process.

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