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# IMPLEMENTATION OF A PROTOTYPE ADSL SYSTEM USING TI TMS320C6X DSP

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## ABSTRACT

*The Asymmetric Digital Subscriber Line (ADSL) is a local loop transmission technology that simultaneously transports downstream (towards customer) bit rates of up to 8 Mbps, and upstream (towards network) bit rates of up to 800 kbps, and plain old telephone service (POTS) via a single pair of wires. The increased bandwidth available allows real-time applications like video-on-demand (VOD) live video conferencing and remote Local Area Network (LAN) access to be accessible via the public switched telephone network.*

*This paper discusses the implementation of a prototype ADSL system on the Texas Instruments TMS320C6701 Digital Signal Processor Evaluation Module. The software blocks were coded and optimized in ANSI C and downloaded into the target system. A simplified frequency scaled model of the subscriber loop is used as the channel in testing the system in loop back mode. An online bit error rate test sequence was performed to determine system performance. An aggregate bit rate of 66.15 kbps with a bit error rate (BER) of appoximately $10^{-7}$ was achieved.*

## I. Introduction

The Philippines at present is showing a steadily increasing desire for greater bandwidth. More and more Filipinos are using the Internet for business, research, communication, information access, and recreation. A typical residential consumer accesses the Internet through dial-up connections with the use of voiceband modems attached to the local phone line. This method of information transfer can achieve a maximum of only 56 kbps. The key players in the local telecommunications industry has also recently introduced cable modems as an alternative access medium that can achieve data rates up to 1.5 Mbps.

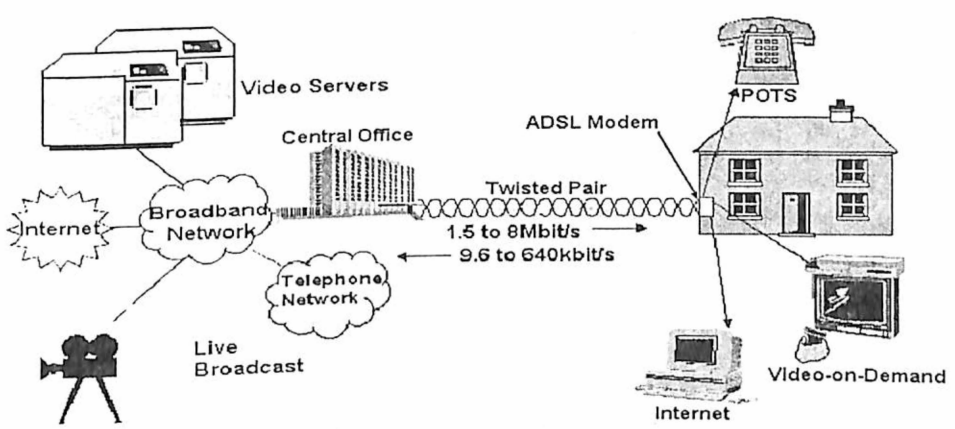
An alternative to the cable modem is the ADSL. This access technology can achieve generally higher transmission rates using the well-established telephone infrastructure as the medium. ADSL operates beyond voiceband frequencies and can achieve downstream data rates of up to 8 Mbps, upstream bit rates of up to 800 kbps, plus telephone service simultaneously via a single pair of wires. This asymmetric allocation of bandwidth is meant to take advantage of the majority of high bandwidth applications like high-speed Internet access, video-conferencing and video-on-demand.

A typical network infrastructure based on ADSL is presented in Figure 1. The left side of the figure shows a broadband network that interconnects the various applications possible, e.g.

Internet, Video-on-Demand servers, Live Broadcast TV, and Plain Old Telephone Service. These are all connected to the Central Office of a Telephone Company that has ADSL Central Office modems that multiplex all the data and transmit it through regular copper twisted pairs towards the residential consumer. The residential consumer shall then have an ADSL Remote Terminal modem that allows him to access the applications that were mentioned. This huge bandwidth is possible because ADSL utilizes the higher frequencies, i.e., 4kHz – 1.1 MHz that is achievable in a typical copper loop and modulates the data using sophisticated coding and signal processing techniques.

Extensive research on ADSL has already been done in recent years. Different companies in the United States and Europe have already started to make this service available to residential consumers. The American National Standard Institute (ANSI) has also published standards on ADSL [1]. However, there is still a lot of room for further research. The high complexity of the modulation and demodulation methods have always made research and development and manufacturing costs very high and therefore cause the service to be quite expensive. This is a very big impediment for extensive deployment here in the Philippines.

This research therefore has the purpose of establishing a significant knowledge base on the implementation of ADSL. The research focuses on understanding the core theoretical concepts and applying it to a prototype ADSL system. The functional blocks of the system were separately analyzed, coded and optimized for speed in ANSI C. The optimized code is then downloaded into the TI TMS320C6701 evaluation module and finally tested for performance. The prototype system was able to achieve 66.15 kbps in loop back mode with a bit error rate of appoximately $10^{-7}$.




[1]**Figure 1**. Typical ADSL network infrastructure

[1] Figure used with permission from ADSL forum

## ADSL Fundamentals

The ADSL modem passes through two major states. The first state is the initialization and the second state is the actual exchange of data. In the first state, all the parameters of the functional blocks of the modem are conditioned to support reliable transmission and reception of data. This state is further subdivided into five stages. These are activation, gain setting, synchronization, channel identification and equalizer training. The state and block diagrams of the whole system are provided in Figure 1 and Figure 2 respectively [1].

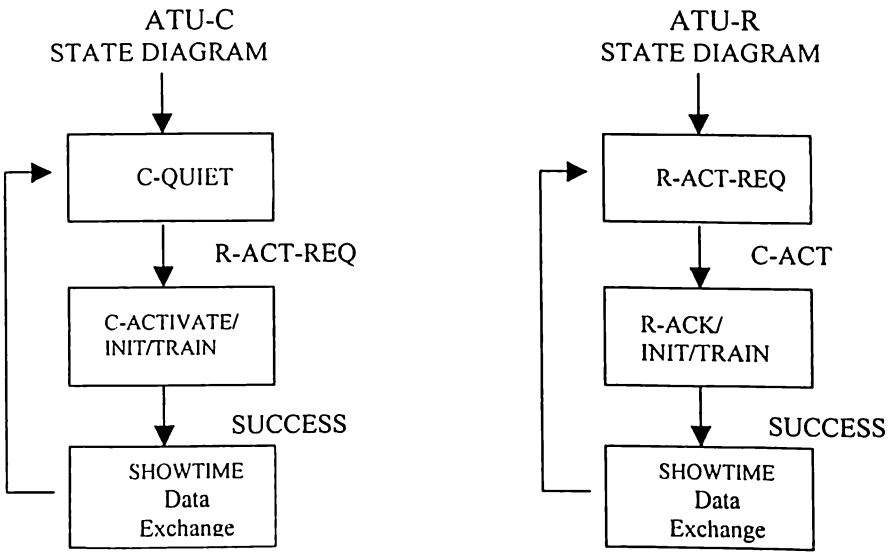



**Figure 2.** State Diagram of the Initialization of the ADSL System.

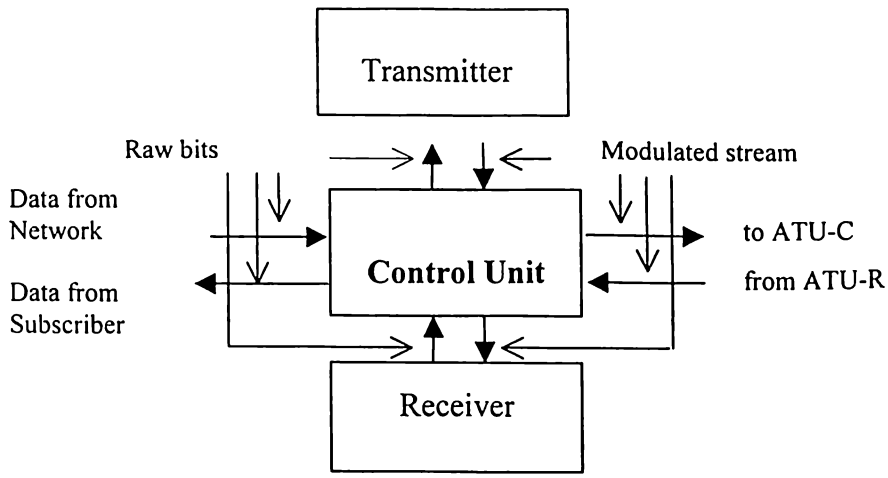



**Figure 3.** Block Diagram of the ADSL System.

The ADSL Transceiver Unit - Remote Terminal (ATU-R) will transmit an activate-request signal to the ADSL Transceiver Unit – Central Office (ATU-C) while the ATU-C is in the C-QUIET State. The ATU-C will then recognize the request and respond. This stage is called activation. When both modems have acknowledged each other, initialization can continue.

The next stage in the initialization is the gain setting. Gain setting refers to the adjustment of the transmit power and of the receiver gain. Performing gain adjustment will minimize the occurrence of quantization errors and of clipping. Both the ATU-R and the ATU-C perform gain initialization.

After setting the gains of the transceivers, the ATU-R will send a signal to the ATU-C requesting for a reference signal that will be used in the identification of the signal-to-noise ratio (SNR) of the channel with respect to the frequency. This is the channel analysis phase. The ATU-C's channel analysis will follow that of the ATU-R.

After the ATU-C's channel analysis, the ATU-C will signal the ATU-R to get ready to receive another signal that will be used to reduce the phase error between the ATU-R's clock and the ATU-C's clock. This stage is the synchronization or symbol timing recovery phase. The final phase will involve a training signal that will update the filter coefficients of the equalizer [2].

The next major phase of the ADSL transceiver communication is the actual exchange of data. Figure 3 and Figure 4 presents a general block diagram of the transmitter and of the receiver.

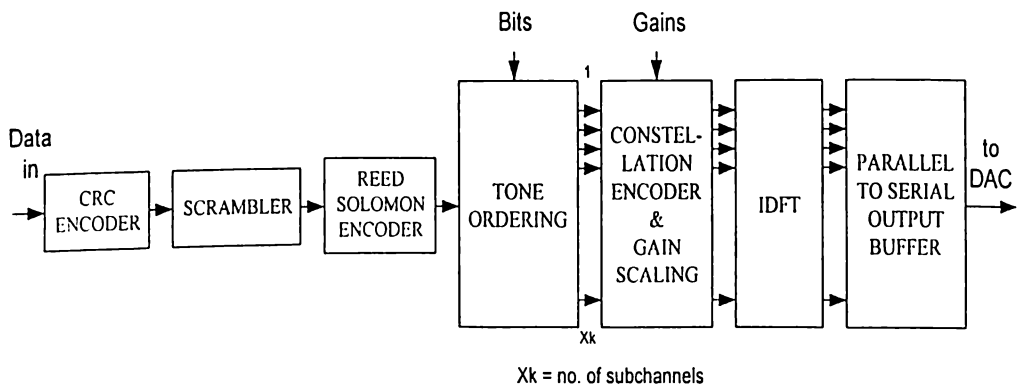



**Figure 4.** Block Diagram of ATU-C Transmitter for STM Transport [1].

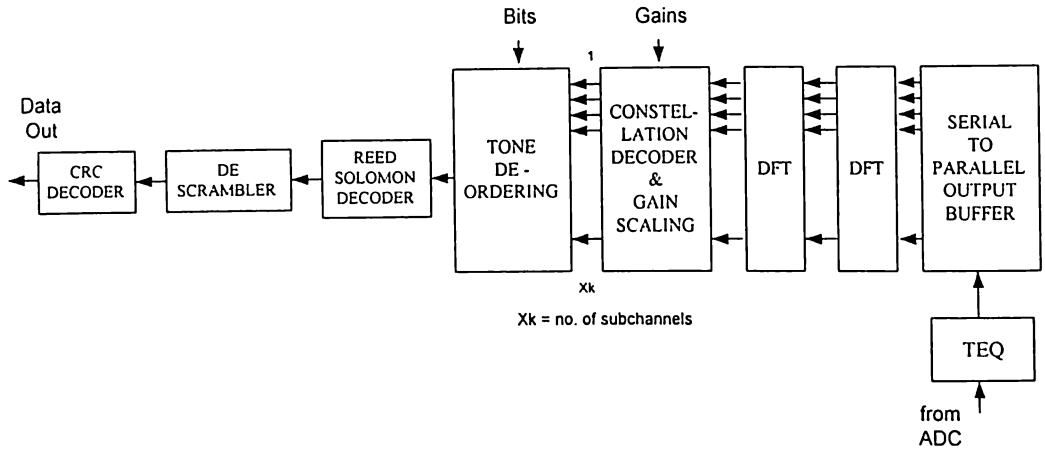



**Figure 5.** Block Diagram of ATU-C Receiver for STM Transport [1].

The receiver is the opposite of the transmitter. For us to understand the operation of both, we first need to know the operation of the transmitter. First, the data stream enters the cyclic redundancy check (CRC) encoding block. Then it goes through the scrambler and passes through the Reed-Solomon (RS) forward error correction (FEC) encoder. The CRC and RS FEC are blocks in the transmitter that add bits in our data stream for error detection and correction [2].

Scramblers in data transmission are used with the hope of "randomizing" an input bit stream. Because strings of zeros or ones may occur in realistic data transfer more often than other strings, it is desirable to make such events less probable. This process helps DSL digital signal processing algorithms to see more robust data and usually prevents DSL subsystems from locking into an undesirable setting that might be caused by highly redundant data. Equalizers, channel-identification methods and timing-recovery loops all often benefit from the use of a scrambler. After performing error control on the input data stream, we prepare our data for analog transmission by applying discrete multi-tone (DMT) modulation.

ADSL modems use wider transmission bandwidth compared to voice band modems. With DMT, our transmission bandwidth is subdivided into sub channels. This partitioning into narrowband sub channels is a solution, originally proposed by Shannon, that reduces inter-symbol interference (ISI). By reducing ISI, we will have simpler implementations of equalizers [2].

The first block of DMT is tone ordering. The SNR of our channel is derived during initialization to determine how much information can be accommodated in a sub channel. The number of bits and relative gains for every tone is calculated in the receiver and passed to the transmitter according to a defined protocol. The pair of numbers ("bits" and "gains") is typically stored in ascending order of frequency or tone number in a bit and gain table.

Tone ordering partitions our data streams into groups of bits that will be carried by a particular sub channel. Grouping bits together prepares our data for constellation encoding. The outputs of the constellation encoder block are sets of gains and phases that are passed to the equalizer of every sub channel. Then, the set of outputs of the equalizer block is given to the Inverse Discrete Fourier Transform (IDFT) for modulation. The IDFT transforms the input data, that are in frequency domain, to data in time domain. Since the output of IDFT is a combination of sinusoids in the time domain, we can already send them to the digital to analog converter (DAC) for analog transmission [2].

As mentioned, the receiver performs the opposite functions of the transmitter with the addition of two blocks: Time-Domain Equalizer (TEQ) and the Frequency-Domain Equalizer (FEQ). Both the TEQ and the FEQ are important in DMT demodulation because they help compensate for the channel distortion. The TEQ is an FIR filter that shortens the impulse response of the channel to increase the efficiency of transmission while making the reception of data reliable. The purpose of the FEQ is solely that of scaling and rotating the constellation on each sub channel so that a common decision device (or decoder) can be used on all sub channels. It is important to note that the FEQ is not really an equalizer in this case, but a device that inverts the channel and thus rotates the phase to zero. All sub channels can then use a common decoder with common assumed spacing of points in the constellations on each sub channel.

## Design Considerations

### *Hardware Subsystem*

The TMS320C6701 ('C67x) evaluation module (EVM) is the core hardware of the system. Aside from the digital signal processor, three peripherals were used to bridge the gap between discrete data and analog signal. The CS4231A 16-bit stereo audio codec serves as the digital-to-analog (D/A) and analog-to-digital (A/D) converter of the modem. The maximum sampling rate of this codec is 48.0 kHz but we used 44.1 kHz for the sampling rate of our modem. At that stage, the availability of hardware resource was one of the reasons that led to the scaled-down implementation of the ADSL system. A sampling rate of 44.1 kHz will imply a maximum operating frequency of 22.05 kHz.

The audio codec has another limitation that is a disadvantage for digital communication, its sampling phase is not adjustable. This means that two 'C67x EVMs cannot be used because the sampling phase of the transmitting module cannot be recovered in the receiving module. Hence correct data cannot be recovered due to a lack of synchronization. Therefore, in the first phase of our development we implemented a loop back system to test the functionality of the modulation and coding blocks.

For our loop back test, we send discrete data through the codec then to the twisted pair so that the transmitted data can at least be subjected to the non-idealities of the channel. After passing through the channel, the data is received on the same evaluation module. It is then sampled, demodulated, and decoded. The processed received data is compared to the pseudorandom data transmitted. The number of errors detected in the received data is accumulated on a counter variable so that at the end of a number of iteration of transmission and reception, the bit error rate of the system will be computed.

The 16-bit sampled data buffered in the codec is sent to the 'C67x chip through a second peripheral called the multi-channel buffered serial port (McBSP). This peripheral is a high-speed serial-to-parallel and parallel-to-serial port that interfaces a device external to the 'C67x DSP chip. The McBSP is connected to the central processing unit (CPU), on-chip memory, and other on-chip peripherals through the memory bus of the DSP chip.

The data coming from Mcbsp is transferred to the on-chip memory by the CPU or by the direct memory access controller (DMA), the third peripheral. If the CPU performed the transfer, the process is called a blocking process. This is so because the cycles that could have been used by the CPU for computation and data processing were used in the transfer of data. During block transfers of data, the use of DMA is more efficient. The DMA, after being prompted by the CPU, takes care of the transfer of data from a peripheral to the memory or vice versa or from a peripheral to another peripheral. This allows the CPU to perform data processing while transferring other data at the same time. Figure 5 gives us a block diagram layout of the devices used in our ADSL system.

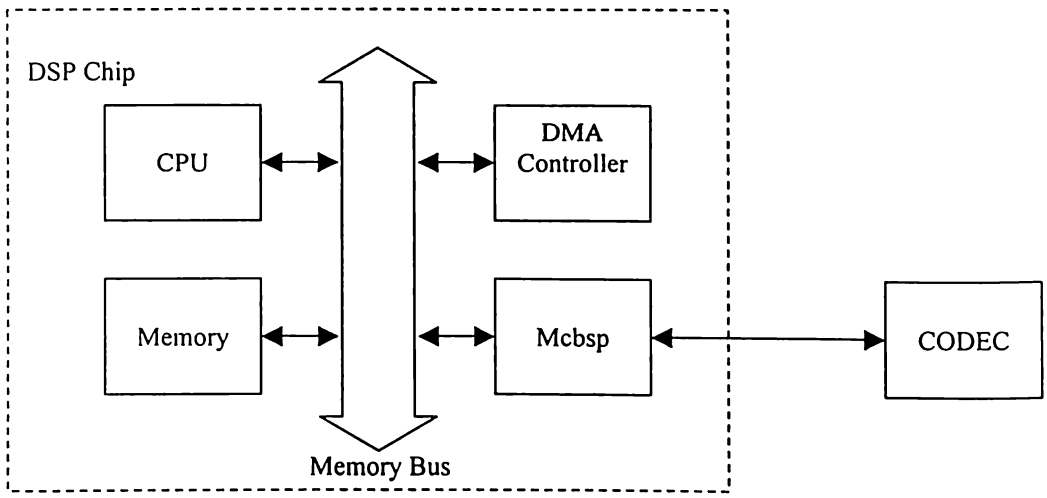



**Figure 6.** EVM Device Layout

## *Software Subsystems*

The development of the prototype ADSL system generally followed the standards presented in the ANSI T1.413 Issue 2 [1]. However, significant parameter deviations were necessary to enable the development of a considerable ADSL Transceiver on the TI TMS320C6701 EVM.

## *Discrete Multitone (DMT) Modulation Parameters*

The ANSI and ITU standards mentioned above both recommend the Discrete Multitone Modulation or DMT as the modulation scheme to be used for ADSL. DMT is basically a multicarrier modulation scheme that employs the Discrete Fourier Transform in order to partition a wide band channel into narrow band and orthogonal channels. A general block diagram of a typical DMT Transmission system is shown in Figure 6.

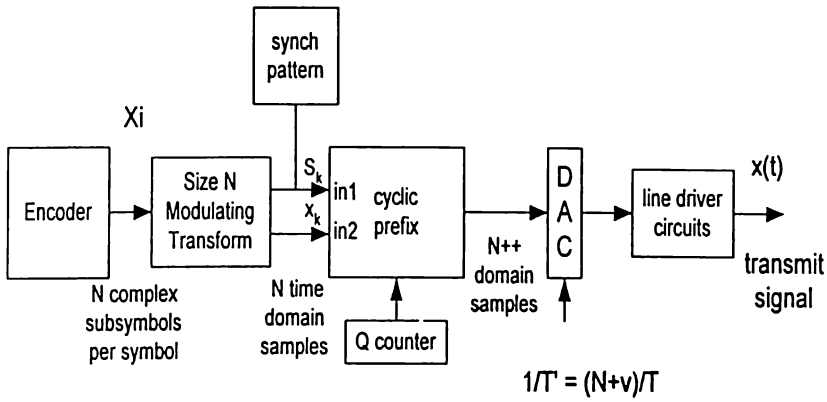



**Figure 7.** DMT Modulator Description [3].

A typical DMT system can generally be characterized by the following 5 parameters:

1. $1/T'$, the **sampling rate, with sample period** $T'$,
2. $N$, the integer size of a complex-to-real Modulation Transform in sample periods,
3. $\nu$, the integer **cyclic prefix length,**
4. $Q$, the integer number of symbols between known "synch symbols,"
5. $\delta\nu$, the integer number ($\pm$) of samples stuffed or robbed in the cyclic prefix of synch symbols.

We shall now refer to Figure 6 to describe these parameters. The symbol period of a DMT system is defined as

$$T = (N + \nu)\, T' \qquad (1)$$

In each symbol period, $N$ complex sub symbols are input to a *Modulating Transform,* which in our case is the IFFT, with a resultant set of $N$ real-valued output samples. The cyclic prefix function prepends a copy of the last $\nu$ samples to the beginning of the sample block to form a symbol of $N + \nu$ samples. A Digital-to-Analog Converter (DAC) with a sampling rate of $1/T'$ then converts these samples to the analog domain. After $Q$ successive data-carrying symbols have been transmitted, one sync symbol of a specified set of samples is transmitted. This symbol can nominally be omitted, but is useful for fast restoration of service if micro or macro interruptions have occurred and can also be used for resynchronization or retraining of equalizers. $\delta\nu$ is an integer variation in the length of the cyclic prefix of the sync symbol, which results to a length of $\nu \pm \delta\nu$ samples for the cyclic prefix.

It can be shown that it is most desirable to have the symbol period of the multicarrier signal as long as possible [4]. The main limitation, however, is the permitted data delay, $T_{del}$, or latency through a modem. In a carefully designed DMT system, the latency is at least 3 symbol periods, therefore

$$T < T_{del} / 3 \qquad (2)$$

The next choice would be the maximum transmission frequency, $f_{max}$, that may be needed through any channel and for any data rate envisioned for the system. This defines the sampling rate, $f_{samp}$ for the system and the size $N$ of the IFFT/FFT:

$$f_{samp} > 2 f_{max} \tag{3}$$

and $$N = 2^M > f_{samp} T \tag{4}$$

The researchers assumed an acceptable $T_{del}$ to be 10 msec, therefore the symbol period $T$ must be less than 3.33 msec. A significant design constraint for the system would be the on-board voice band codec (CS4231) that has only the following allowable sampling rates in kHz: 5.5125, 6.6150, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.4286, 32, 33.075, 37.8, 44.1, and 48. The researchers chose

$$f_{samp} = 44.1 \text{ kHz} \tag{5}$$

because it is the highest, most flexible sampling rate in the sense that it has the most factors within the allowable sampling rates (5.5125, 11.025, 22.05 and 33.075 kHz). Having determined the sampling rate, we have from (2) that

$$f_{max} < 44.1 / 2 = 22.05 \text{ kHz} \tag{6}$$

The next step would be to choose an appropriate $N$ that will determine how many partitions the sampled channel would have. It is recommended in [5] that N be chosen as large as possible to minimize distortion with the constraint that the transceivers have considerable computational complexity knowing that N would be the size of the FFT/IFFT. At the same time, N should also satisfy (4), so the researchers chose

$$N = 128 \tag{7}$$

This means that the frequency spacing of the channels is

$$\Delta f = 44.1 \text{ kHz} / 128 = 344.53125 \tag{8}$$

which follows that

$$T_{mel} = 1 / \Delta f = 2.902 \text{ msec} \tag{9}$$

and the number of sub-channels is given by

$$N' = N/2 = 64 \tag{10}$$

Figure 3-3 depicts the DMT transmission spectrum. Essentially, 64 sub-channels of 344.53125 Hz wide tones each carry a fraction of an aggregate data rate.

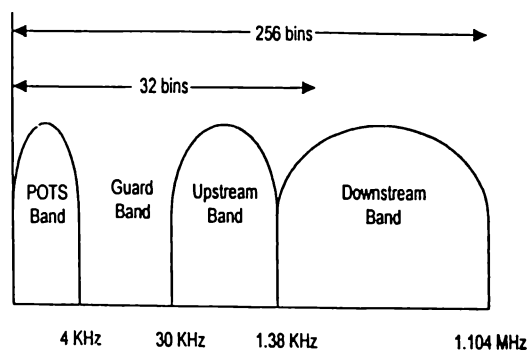



**Figure 8.** DMT Transmission Spectrum

The next parameter to be determined is the cyclic prefix length ν making sure that T satisfies (2) and is short enough such that the efficiency N / (N+ν) is within considerable bounds. The researcher choose

$$\nu = 12 \tag{11}$$

which follows that

$$T = (128 + 12) / 44.1 \text{ kHz} = 3.17 \text{ msec} < 3.33 \text{ msec} \tag{12}$$

The fourth and fifth parameters, which pertain to framing considerations, were omitted in the design for simplicity. These parameters are used for synchronization purposes in practical systems. Since the prototype system uses a loop back testing configuration, on line synchronization is no longer necessary.

Aside from the 5 parameters that characterize a DMT system, other parameters are also needed to complete the ADSL specification. The first of these is the maximum bit allocation, $b_{max}$, per sub-channel. The researchers chose to adapt the G.lite standard of having

$$b_{max} = 8 \text{ bits} \tag{13}$$

as the maximum bit allocation thereby having the $2^8 = 256$ point constellation as the largest. Since the main purpose of the project is not really to achieve the highest data rates, keeping the maximum constellation size to a manageable level in terms of computational complexity and memory requirements is a good strategy.

The parameters discussed above are only for one direction of transmission. It is a significant design deviation from actual ADSL systems, which need different DMT parameters for the two transmission directions, contributing to the asymmetry in data rates. The derivation for the lower bandwidth upstream channel would parallel the above discussion and is included in the following summary of parameters for future reference.

| Parameter Name | Symbol | Downstream | Upstream |
|---|---|---|---|
| Sampling rate | T' | 44.1 kHz | 22.05 kHz |
| FFT/IFFT length | N | 128 | 64 |
| Number of Sub channels | N' | 64 | 32 |
| Frequency spacing | Δf | 344.53125 Hz | 344.53125 Hz |
| Length of cyclic prefix | ν | 12 samples | 6 samples |
| Maximum bit/channel | $b_{max}$ | 8 | 8 |

**Table 1.** ADSL DMT Modulation Parameters.

## DMT Demodulation

A typical DMT demodulator has the daunting task of decoding the transmitted signal after passing through a highly distorting channel such as the telephone twisted pair. It is therefore very important to design the demodulator carefully in order to achieve the data rates promised by the ADSL system. A typical DMT demodulator is shown in Figure 8.

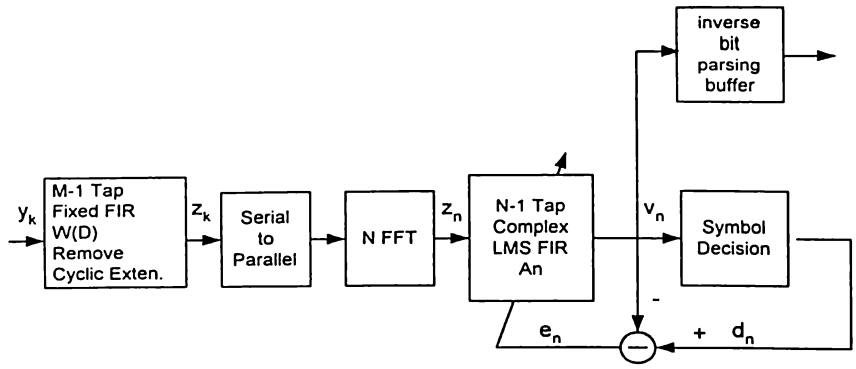



**Figure 9.** A Typical DMT Demodulator [4].

A typical DMT DMT receiver consists of an Analog-to-Digital Converter (ADC), Time-Domain Equalizer (TEQ), serial to parallel conversion, FFT, Frequency-Domain Equalizer (FEQ), symbol and bit decisions and the inverse parsing functions.

After the ADC, the received signal is first filtered by the TEQ, which is typically an adaptive FIR filter. The purpose of the TEQ is to shorten the effective impulse response of the channel to fit the region of the cyclic prefix guard band. The length of the cyclic prefix, $\nu$, was previously designed to be 12 samples long, therefore the length of the target channel, $L_b$ is also set as

$$L_b = 12 \tag{14}$$

The length of the TEQ, $L_w$, on the other hand, is set to

$$L_w = 32 \tag{15}$$

which is typical for an ADSL system [4].

After the TEQ, the samples corresponding to the guard period cyclic prefix are dropped, which is eventually inputted to the FFT after serial to parallel conversion. The FEQ, which is typically an N-1 tap complex FIR filter, is then used to correct both magnitude and phase distortion of the equalized channel when using a single decision device for all the sub channels. The FEQ is designed similar to a Frequency LMS where the equations used are indicated in Sec. 2.2.5. The crucial parameter in LMS algorithms is the step parameter $\mu$, which, by trial and error, was set as

$$\mu = 0.1 \tag{16}$$

After the FEQ, the symbol is then decided upon and the bits decoded for final inverse parsing. The transmitted data is then successfully received.

## Error Control Blocks

In designing the error control blocks, it is important to know the allowable size of data bits per transmission of symbol to determine the ranges of overhead. There are 64 tones each for both the upstream and the downstream channels. The minimum number of bits per tone is 2. This means that the minimum number of bits per symbol is $2 \bullet 64 = 128$. The other consideration here is that the number of data bits should be word-aligned or should be a factor of 32. 128 is divisible by 32 but we have to consider the fixed 8 CRC bits. This means that the minimum

number of bits per symbol is 136 bits. The maximum number of bits per symbol is $64 \bullet 8 = 512$. Since we have to account for the overhead while trying to keep the number of bits as a multiple of 32, the maximum number of bits per symbol was limited to 488. The next design consideration is the number of Reed-Solomon bytes. According to the graphs of coding gain versus percentage redundancy at a data rate of 1.6 Mbps in [6], a percentage redundancy ranging from 10% to 25% will produce a relatively high coding gain. This is the basis for the error control coding design consideration. The data rate 1.6 Mbps was chosen since it is the one nearest our scaled down ADSL prototype. Table 3-2 indicates the allowable symbol size in bits.

The CRC block appends eight redundancy bits per symbol using the generator polynomial $X^8 + X^7 + X^2 + 1$. The generator polynomial for the scrambler is $1 + D^{-18} + D^{-23}$ [6]. The Reed-Solomon Forward Error Correction block uses the formula $g(x) = (x-\alpha)(x-\alpha^2)(x-\alpha^3)\ldots(x-\alpha^{2t})$ in coming up with a generator polynomial. The codeword encoded is capable of correcting up to t bytes of erroneous bits.

| Number of Bits Per Symbol | Number of Data Bits | Percentage Redundancy – number of correctable bytes |
|---|---|---|
| 136 | 96 | 23.53% - 2 |
| 168 | 128 | 19.05% - 2 |
| 200 | 160 | 16.00% - 2 |
| 232 | 192 | 13.79% - 2 |
| 264 | 224 | 12.12% - 2 |
| 296 | 256 | 10.81% - 2 |
| 360 | 288 | 17.78% - 4 |
| 392 | 320 | 18.37% - 4 |
| 424 | 352 | 16.98% - 4 |
| 456 | 384 | 15.79% - 4 |
| 488 | 416 | 14.75% - 4 |

**Table 2.** Allowable Symbol Size In bits

## Channel Analysis

Channel identification is necessary for transmission designs that use an equalizer, particularly Decision Feedback Equalizer (DFE) or Time Equalizer (TEQ), and also for DMT. Generally, channel identification methods measure the channel pulse response and noise power spectral density. Multitone channel identification directly estimates signal and noise parameters for each of the sub channels. These parameter estimates will then be fed to some special optimization algorithms that will allocate the amount of information that will be carried by each sub channel.

The ADSL's T1.413 Issue 2 [1] standard suggests a pseudorandom signal with a cyclic prefix as the training signal. It is called C_MEDLEY and is used in the estimation of channel pulse response, signal, and noise parameters.

Gain estimation or pulse response estimation is the first step in the channel analysis. The equation used to obtain the estimate of the pulse response, $\hat{P}_n$ is

$$\hat{P}_n = \frac{1}{L}\sum_{l=1}^{L}\frac{Y_{l,n}}{X_{l,n}} \tag{17}$$

$X$ - the training signal in frequency domain

$Y$ - the received training signal in frequency domain

$n$ - the sub channel number

$L$ - 40 was the suggested number of training symbols [1]

After estimating the pulse response of the channel, we can proceed with the computation of the variance estimate, $\hat{\sigma}_n^2$.

$$\hat{\sigma}_n^2 = \frac{1}{L}\sum_{l=1}^{L}\left|E_{l,n}\right|^2 \tag{18}$$

where

$$E_{l,n} = Y_{l,n} - \hat{P}_n \cdot X_n \tag{19}$$

$E$ - the error signal in frequency domain

$L$ - 3200 was the suggested number of training symbols to ensure that the excess noise in the estimate of noise will be less than 0.1 dB [1]

The availability of the channel pulse response estimate will enable us to compute for the gain parameters needed by the encoder/decoder of the DMT. Equation (4-25) is used to compute for the gain parameters.

$$g_n = \left|\hat{P}_n\right|^2 \tag{20}$$

The last part of the channel analysis will enable us to obtain the bit capacity of every sub channel through the use of Campello's Efficiency (EF) and E-Tightness (ET) algorithms [1]. These are rate-adaptive algorithms employed in Rate Adaptive DSLs (RADSL).

Initially, the algorithms start with any unit of information vector $\bar{B}$ whose components sum to the total bit capacity, $B$, of the channel. Equations (4-26) and (4-27) are the incremental energy cost to increase from $B_i$ to $B_i + 1$ units of information and transmit energy for sub channel i. These equations are used in the algorithms that follow.

$$e_i(B_i) = \frac{2^{B_i}\cdot\Gamma\cdot\hat{\sigma}_i^2}{\left|\hat{P}_i^2\right|} \tag{21}$$

$$\varepsilon_i = \frac{2^{B_i}-1}{\left|\hat{P}_i^2\right|}\cdot\Gamma\cdot\hat{\sigma}_i^2 \tag{22}$$

$\Gamma$ - 3 dB is the system design SNR-gap

Campello's solution to Rate-Adaptive Loading:

1. Choose any $\bar{B}$

2. Make $\vec{B}$ efficient with EF algorithm
3. E-tighten $\vec{B}$ with ET algorithm

The detailed procedure of EF and ET algorithms are outlined in [6].

## Performance

The following results were acquired from our loop back test:

- Bit rate of 66.15 kbps
- Baud rate of 344.53 symbols/sec
- Bit error rate of $10^{-7}$

During the channel characterization the graphs of the noise response, pulse response and sub channel bit allocation were plotted. These plots are shown in figure 9, 10, and 11.

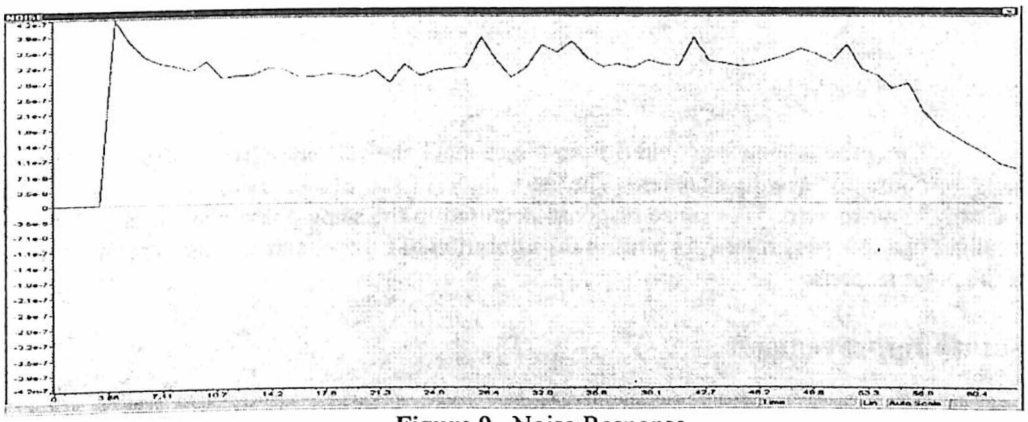


**Figure 9.** Noise Response

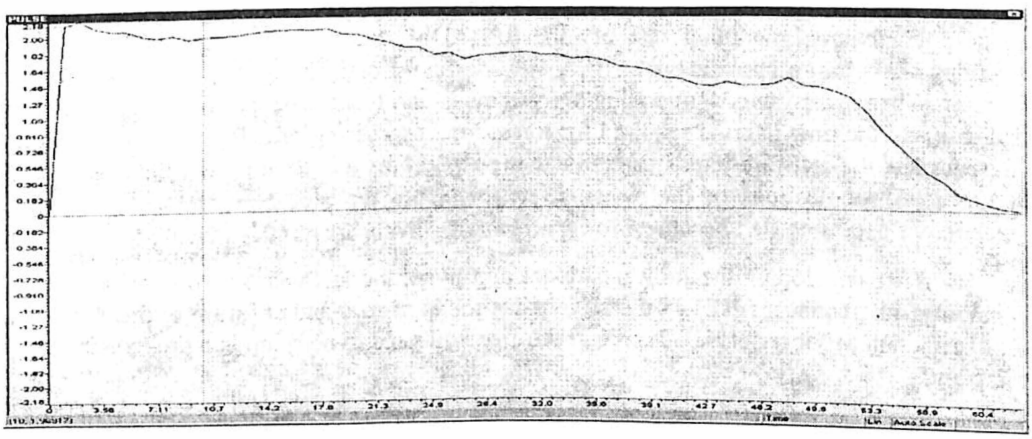


**Figure 10.** Pulse Response

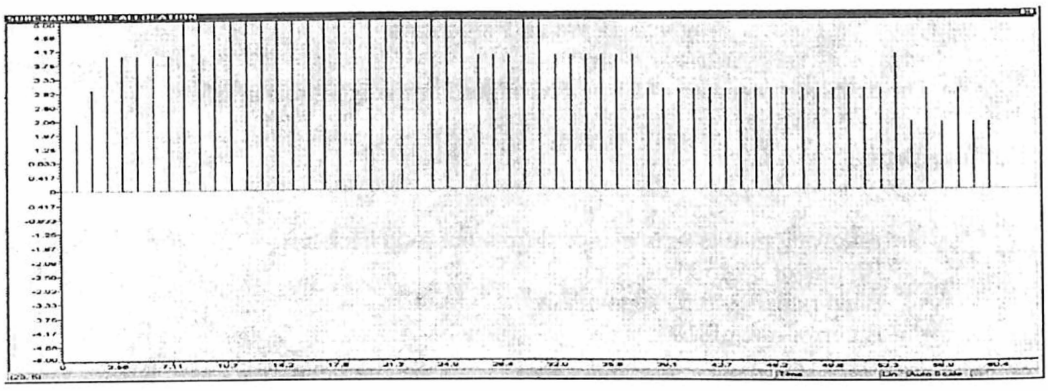


**Figure 11.** Sub channel Bit Allocation

The noise response acquired from the channel analysis phase resembles a white gaussian noise response for a wire channel. The magnitude of the highest peak is $4.2 \times 10^{-7}$ which is basically close to zero. The pulse response acquired in the same phase decreases with frequency resulting in a low pass filter. As a result the allocation of bits per sub channel resembles the shape of the pulse response.

## Future Improvements

At this stage we have finished testing the algorithms for modulation and coding. But improvements must be made to make the prototype fully functional. The first thing that should be done is to acquire a daughter board from a third party support so that the analog interface with the public switched telephone network (PSTN) will be supported. The daughter board should also support the required sampling rate of the full ADSL system and should have an adjustable sampling phase for synchronization.

When the system's operating frequency is increased, the period of one symbol will decrease and the time interval required for a real-time processing of data will also decrease. As a consequence, the software implementation of the algorithms will have to be optimized to conform to the new specifications of the system. At this stage the protocols of the transmission and reception of data is needed because two separate transceivers are already involved.

After developing the fully functional prototype, the last phase is to develop a peripheral component interconnect (PCI) card that contains the hardware and software of the ADSL modem for distribution to subscribers. Then central office will need to be setup in a pre-existing telephone company.

The last phase is something optional because before it can be pursued one has to assess and compare the cost of setting up a locally produced to an internationally produced ADSL system.

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