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THERMAL MANAGEMENT IN ELECTRONIC PACKAGES

Manolo G. Mena
Professor and Chairman
Department of Mining and Metallurgical Engineering
College of Engineering
University of the Philippines
Diliman, Quezon City, Philippines

ABSTRACT

Packaging of an integrated circuit not only involves the physical isolation of the delicate integrated circuit or "silicon chip" from the environment but also the provision of a thermal conduction path to allow the heat generated during the operation of the chip to be dissipated to the environment. This paper presents the various types of failures accelerated by an increase in temperature of the integrated circuit and the modes of heat transfer through the packaging material. Characterization of the thermal characteristics of IC packages through the use of "thermal resistances" in also presented.

INTRODUCTION

The temperature on the surface of a semiconductor device or chip depends on the total thermal resistance between the die, its external environment and the device power dissipation. The demand for faster and higher performance in integrated circuits has led to an increase in power dissipation per circuit as well as an increase in the number of circuit and circuit density on the surface of the silicon chip. The overall effect is an increase in power density of devices, i.e., more heat being generated. The power density has been increasing exponentially with time for the past twenty years. On the other hand, the drive towards miniaturization has resulted in smaller packages, with decreased area for heat dissipation. The net effect is that devices now run at much higher temperatures than their predecessors.

Thermal management is the method by which the temperature of an operating device is kept below the maximum allowed temperature. Operating at higher temperatures can result into catastrophic failures as well as jeopardize the long term reliability of the device as well as the electronic package.

This paper analyzes the failures caused by operating at excessive temperatures, the mechanisms of heat transfer in electronic packages as well as the factors and solutions that affect the transfer of heat from the silicon die.

FAILURES ACCELERATED BY HEAT

Failure mechanisms in electronic components are kinetic in nature and are exponential functions of temperature, as predicted by Eyrings equation:

$$\mathrm{Rate}(T_2) = \mathrm{Rate}(T_1)\exp[E/k(T_2^{-1}-T_1^{-1})] \qquad (1)$$

where K is Boltzmann's constant and E is the activation energy of the particular failure mechanism. Thus, an increase in temperature results in an exponential increase in the failure rate. Should the temperature exceed certain material properties, this could also result in catastrophic failure. Discussed below are some of the various catastrophic and reliability concerns accelerated by temperature.

Electromigration

Electromigration involves the transport of metalization atoms from regions of high current flow to regions of low current flow. Ultimate failure of the device could either be shorting of metal lines in areas where metal atoms deposit (called Hillocks) or metal opens in the high current flow region due to the coalescence of vacancies created by the migrating atoms into voids and eventually into an "open". The failure rate is a power function of the current density and an exponential function of temperature as shown in the equation below:

$$\text{Failure Rate} = Aj^n \exp(-E/kT) \qquad (2)$$

where n = adjustable integer constant from 1 to 7
A = constant
E = activation energy, 0.5-0.7 eV
m = current density
k = Boltzmann's constant.

Contact Failure

Contact failure refers to the breakdown in electrical continuity at the metal-silicon interface due to the generation of voids at the contact area, a phenomenon similar to electromigration or the deposition of retifying silicon precipitates. The failure is both current and temperature dependent, as shown below:

$$\text{Failure Rate} = Am^n \exp(-E/kT) \qquad (3)$$

where n = adjustable integer constant from 1 to 7
A = constant
E = activation energy, 0.9 eV
m = current density
k = Boltzmann's constant.

Dielectric Breakdown

Dielectric breakdown involves the decomposition of dielectric of insulating layers, which are commonly either oxides or nitrides of silicon as a function of temperature and electric field, as shown by the equation below:

$$\text{Failure Rate} = A\exp\{(-E/kT)+CV\} \qquad (4)$$

where A,C = constants
E = activation energy,0.3-1eV, depending of root cause
K = Boltzmann's constant.

Corrosion

Corrosion involves the electrochemical degradation of metalization, aluminum in particular on the surface of the die. Corrosion is accelerated both by the relative humidity the package is exposed to and its operating temperature, as shown by the following equation:

$$\text{Failure Rate} = A(RH)^{-2.66}\exp(-E/kT) \qquad (5)$$

where A = constant
RH = relative humidity
E = activation energy, 0.8 eV

Intermetallic Growth

Intermetallic growth refers to the growth of aluminum-gold intermetallics in ball bonding and tin-copper intermetallics in plated copper leads. Gold-aluminum intermetallic formation is accompanied by the formation of Kirkendall voids due to the higher diffusivity of aluminum into gold. Excessive Kirkendall voiding results into higher electrical resistance and mechanical degradation of the bond which could open by lifting under normal operating conditions. Rate of failure due to Kirkendall voiding is solely a function of temperature as shown below:

$$\text{Failure Rate} = A\exp(-E/kT) \qquad (5)$$

where A = constant
E = activation energy, 1.0 eV

Growth of the tin-copper intermetallic results in the consumption of the tin on plated copper parts. This intermetallic provides a non-solderable surface to final board assembly of the parts. Failure rate is of the same form as equation (5), with the activation energy being equal to 0.5 eV.

Fatigue

Fatigue failure occurs when mechanical and/or thermal loading causes repetitive tensile and compressive stresses to occur inside the package. Metallic components, e.g. bonding wires and aluminum metalization in the package are normally in jeopardy and the absolute value of the stress is generally way below the ultimate strength of the material. Ultimate failure of the material is an open circuit due to the rupture of the wire or metalization. The number of cycles to failure is modeled by the equation:

$$\text{Cycles to Failure} = (A/\Delta\gamma)^{m} f^{n} \exp(-\beta/kT\mathrm{max}) \qquad (6)$$

where A = cross-sectional area of metal component
f = cycling frequency
m, n, β = empirical constants,
$\Delta\gamma$ = plastic strain, and
k = Boltzmann's constant.

Creep

Creep involves the plastic deformation of metal lines on the surface of the device due to the sustained application of low level stresses at elevated temperatures. Device failure occurs when deformed metal line short in areas of close metal line spacing. The following equation is used to model rate of failure as a function of the applied stress and temperature:

$$\text{Failure Rate} = A\sigma^{n} \exp(-E/kT) \qquad (7)$$

where A, n = empirical constants,
σ = applied stress,
E = activation energy, 0.8 eV,
k = Boltzmann's constant.

Die and Package Cracking

Thermomechanical stresses are generated in composite materials due to the differences in the coefficients of thermal expansion (CTE) between component materials. In general, the maximum shear stress level is directly proportional to the difference in CTE, the temperature range and the geometric average of the moduli of elasticity:

$$\sigma\text{max} = A(\Delta\alpha)\ (\Delta T)(E_1E_2)^{1/2} \qquad (8)$$

where A = constant,
$\Delta\alpha$ = difference in CTE,
ΔT = difference in temperature,
E_1E_2 = moduli of elasticity.

An added complication is the degradation of mechanical properties as temperature increases such that the thermomechanical stress could exceed the fracture strength of the material at that particular temperature.

PACKAGE THERMAL CHARACTERISTICS

Modes of Heat Transfer

In a packaged IC, the heat dissipated at the die as a result of the conversion of electricity to heat is transferred to the package exterior by conduction. Conduction is the transfer of heat from one part of the body to another part of the body or a second body in physical contact with the first. Simply stated, conduction is heat transfer through a solid medium. The rate at which heat transfer by conduction occurs is quantified through Fourier's Law which states that the rate of heat flow is proportional to the thermal gradient, with the proportionality constant being the thermal conductivity of the material:

$$q = -k(dT/dx) \qquad (9)$$

where q is the rate of heat transfer per unit area per unit time.

Heat is also transferred from the package through the metal leadframe to the printed circuit board by conduction. The amount of heat dissipated through this route is directly proportional to the distance between the die pad and the lead tip, the number of leads in a device, metal used and the physical dimension of the lead. Shown in Table 1 is a summary of the thermal conductivities of common IC packaging materials.

Convection involved the transfer of heat from a solid to the fluid around it, or heat transfer through a fluid medium. Mechanistically, convection is actually heat conduction through a stagnant fluid layer around a solid. Unfortunately, the determination of the thermal conductivity as well as the thickness of this stagnant layer is extremely difficult that these variables are lumped together in a convective heat transfer coefficient. Fluid dynamics reveals that the thickness of this stagnant layer is a direct function of the characteristics of the flow, as defined by four (4) dimensionless numbers: Reynolds, Grashof, Prandtl and Nusselt numbers. The objective of such dimensionless number manipulations is the identification of the appropriate heat transfer coefficient which goes directly into Newtons' Law of Cooling which states that:

$$q = h(Ts - Ta) \tag{10}$$

where h = convective heat transfer coefficient,
Ts = surface temperature, and
Ta = ambient temperature.

Radiation is heat transfer in the absence of a medium and is quantitatively determined using Stefan-Boltzmann's equation:

$$q = \varepsilon\delta(Ts^4 - Ta^4) \tag{11}$$

where ε = emissivity of the surface,
δ = Stefan-Boltzmann's constant ($5.67\times10^{-8}W/m^2$-°K),
Ts = surface temperature,
Ta = ambient temperature.

Relative Magnitudes of Heat Transfer Mechanisms

An approximation of the relative magnitudes of heat transferred through the mechanisms described above may be done by considering a package with a maximum case temperature of 85 °C (industrial application; commercial is 70°C and military is 125°C) and an ambient temperature of 25°C. Calculating the heat transfer by conduction for alloy 42 (k=20 W/m-C) and for copper (k=390 W/m-C) leadframes using Fourier's Law, the following values are obtained:

q(alloy 42) = 120 W/cm^2 for a mm thick substrate, and

q(copper) = 2,340 W/cm^2 for a mm thick substrate.

For convective heat transfer assuming a planar surface, the heat transfer coefficients are as follows:

h = 1 m W/cm^2 for natural convection, and

h = 30 mW/cm^2 for forced air convection.

Using Newton's Law of Cooling, the convective heat transfer rate is estimated to be:

q = 60 mW/cm^2 for natural convection, and

q = 1.8 W/cm^2 for forced air convection.

Heat transfer by radiation is a direct function of the surface temperature and for a body with an emissivity of unit at 85°C and an ambient temperature of 25°C,

$$q = 44\ \mathrm{mW/cm^2}$$

This simplistic view of the heat transfer mechanisms show that radiative heat transfer only becomes significant if the leadframe material has low thermal conductivity, as in alloy 42 and under natural convection conditions. For packages with copper leadframes, heat transfer is basically by conduction and convection. To determine the actual distribution in this case requires detailed modeling for specific package types using Finite Element Analysis.

Table 1. Thermal Conductivity of Packaging Materials at 25°C.

Material	W/m-K
Alloy 42 (Fe, Ni)	20
Aluminum	240
Alumina	21
Copper	390
Epoxy die attach	1
FR 4 board	0.2
Molding compound (silica filled)	0.66
Molding compound (alumina filled)	155
Molding compound (Al-Nitride)	150
Gold	297
Kovar (Fe, Ni, Co)	17
Metal Solder (Au-Sn)	57
Metal Solder (Sn-Pb)	36
Silica	1
Silicon	84
Silver	418

Thermal Resistance of IC Packages

A simplified approach based on one-dimensional heat flow and lumped parameters is used in the industry to characterize the thermal performance of IC packages. These parameters are defined as follows:

$$\theta ja = (Tj - Ta)/P \tag{12}$$

$$\theta jc = (Tj - Tc)/P \tag{13}$$

$$\theta ja = \theta jc + \theta ca \tag{14}$$

where θja = junction to ambient thermal resistance (°C/W),
θjc = junction to case thermal resistance (°C/W),
Tj = average die surface temperature (°C),

Ta = ambient temperature (°C),
Tc = case surface temperature (°C), and
P = device power dissipation, (W)..

θjc is a measure of the package internal resistance from the silicon die to the package exterior surface. This parameter is strongly dependent on the thermal conductivity of the packaging material and package geometry and is purely thermal conduction in nature. θja, the junction to ambient thermal resistance includes not only package internal resistance but also convective and radiative heat transfer at the package surface. θca is the case to ambient thermal resistance which depends on package geometry, air flow characteristics, temperature of the package surface and the geometric effects of sorrounding components. Obviously, since θja and θca are dependent on ambient conditions, they are not constants and must be specified at systems conditions. Standard test set up configurations are recommended in military, SEMI, and JEDEC specifications for measuring thermal resistances.

PACKAGING SOLUTIONS TO THERMAL CHALLENGES

Packaging Materials

Qjc is basically a function of the thermal conductivities of the packaging materials used and has been the driving force for the conversion of the leadframe material from alloy 42 to copper. Silica fillers are added to molding compounds for enhanced thermal properties, increased fracture resistance and thermal expansion matching with the silicon die. The use of spherical fillers has allowed mold compound suppliers to increase filler loading from 70 to 85%, thus further improving thermal conductivity of the package. More recent work have focused on the use of alumina ($k = 20$ W/m-K) and aluminum nitride ($k = 230$ W/m-K) as filler materials. Alumina is found to be very abrasive and damages mold equipment while aluminum nitride is still in experimental stage. Silver-filled die attach materials are a standard in the industry. Silver filling was initially for electrical backside contact but is now being used more for thermal conduction.

Package Design

The junction to case thermal resistance is a direct function of the distance between the die and the leadframe tip, as well as the area available for heat transfer. Analog's thermal coastline design maximizes the area for heat transfer by using a wavy instead of a straight leadfinger tip while their chip on lead (COL) design brings the leadtips right under the die. Although the COL uses an electrically insulating tape for die attach, the thermal performance of the package is up to 50% better than the standard package. Various ways of reducing Θca include the use of external heat sinks or fins or even small motorized fans sitting right on top of the package for cooling.

CONCLUSIONS

As packages become smaller, making area available for convective and radiative heat transfer smaller, board density gets higher and devices operate hotter, thermal management will continue to become an issue and require from packaging engineers innovative solutions in terms of materials and designs.