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PRECISE FREQUENCY GENERATION WITH DIGITAL MODULATION USING DIRECT DIGITAL SYNTHESIS

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ABSTRACT

Frequency synthesis or generation of baseband continuous wave signals is usually implemented through traditional analog techniques using tuned LC tank circuits, quartz crystals or phase-locked loops. This paper discusses a digital alternative, direct digital synthesis (DDS), and compares it with analog methods. A commercially available DDS chip and the results of a DDS system implemented using it are also presented.

INTRODUCTION

Traditional methods for frequency synthesis have always made use of analog components. The most basic oscillators make use of indicators and capacitors to form tuned tank circuits. For added stability, quartz crystals are used which can provide low-cost, stable fundamental output up to around 20 MHz. To synthesize different frequencies using a single circuit, multiple oscillators or dividers may be used but phase-looked loops (PLL) are more flexible and have a much higher output frequency limit. A compromise has to be made however, when using PLL's, in choosing between frequency settling time and stability. Loop filters of PPL's are also not so easy to design and implement.

There is digital approach to frequency generation, direct digital synthesis, which can provide stable and accurate output frequencies up to around 25 MHz. Using a microprocessor to control a DDS, the desired output can also be easily changed. In addition, digital modulation is also easily implemented.

DIRECT DIGITAL SYNTHESIS (DDS)

A direct digital synthesizer is a frequency synthesizer that produces digitized samples of a sine wave that drive a digital-to-analog converter (DAC). Its method may be likened to a microcontroller accessing a ROM for data by providing certain address bits. (Figure 1) In this case, the address bits would correspond to a certain phase angle, while the data given by the ROM would correspond to the amplitude value of a reference sine wave at that instantaneous

phase angle. When this process is done continuously at a rate provided by a system clock, the simplest output possible would be a sine wave with a frequency range of as low as system clock/2^N (where N is the number of address bits of the ROM) to as high as system clock/2 (since sampling theory states that at least two samples per cycle are required to reconstruct a sampled waveform). The lower limit of the output frequency range is the frequency resolution of the DDS and it is also the reference sine wave frequency of the system.

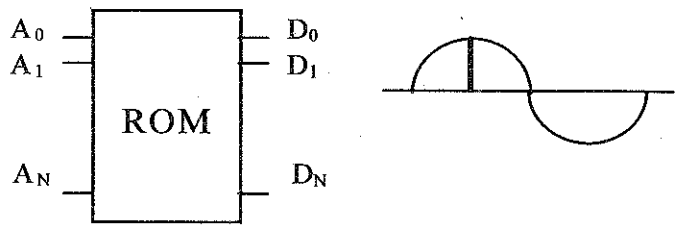

Figure 1. DDS as a microcontroller

Given a specific phase increment, the DDS must be able to automatically increment the input 'address' to the 'ROM' by this phase increment to produce digitized values of the amplitudes. A DAC follows the DDS to convert the digitized values into analog voltages. A low pass filter (LPF) is needed to smoothen the sharp edges of the output waveform from the DAC, which are essentially composed of high frequency components. Since practical filters cannot achieve an abrupt attenuation at the cut-off frequency, an allowance of 10% aside from that of the sampling theorem requirement is made for the maximum output frequency. Thus, the maximum possible output frequency of a DDS is 40% of the system clock.

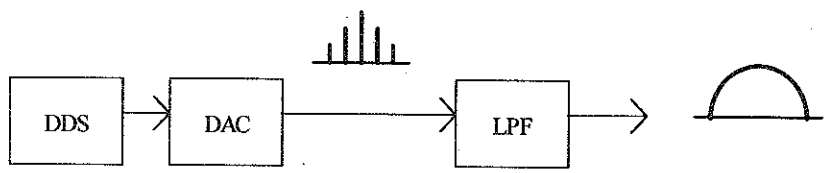

Figure 2. Frequency generation using DDS

As an example, a DDS with a bit resolution of 32 bits is clocked by a 50 MHz system clock. There would thus be 50 million increments by a user-given phase increment value of the 'input address' to the 'ROM' of the DDS every second. The reference frequency would then be 50e6/2^{32} which would be 0.012 Hz. If there were to be a phase increment of one bit (corresponding to a phase angle of 360^0 / 2^{32}) every 20 nsec (period of 50 MHz , obtained by taking its reciprocal), the DDS would produce an output frequency of 0.012 Hz. The highest frequency achievable at the output without distortion would be 50 MHz /2 which is 25 MHz. If

synthesizing of frequencies greater than 25 MHz is done, aliasing would occur. With the LPF taken into consideration, the maximum output frequency would be 20 MHz.

Aside from the simple continuous wave generation, a DDS may be used to produce modulated output. Frequency shift keying is easily achieved by specifying the mark and space frequencies and then simply switching between these two frequencies at the output accordingly with respect to the data. Phase shift keying may also be implemented as long as a proper algorithm is defined to output the proper amplitudes at specific phase angles to produce the phase shifts.

COMPARISON BETWEEN DIRECT DIGITAL SYNTHESIS AND ANALOG FREQUENCY SYNTHESIS TECHNIQUES

As mentioned above, the main advantages of direct digital synthesis over analog frequency synthesis techniques are its very fine output frequency resolution and its fast switching speed. The fine output resolution is easily achieved by using large phase accumulators, usually 32 bits, even as their output is truncated to enable the use of a smaller-sized lookup ROM. Switching between frequencies is fast and straightforward for a DDS because all it entails is writing a new phase increment value into the frequency register of the NCO. In addition, a DDS has a flat and predictable response over a wide output bandwidth (DC to around 25 MHz) and there are minimal analog components that need adjustment or can drift. Digital modulation is implemented easily and outputs of multiple DDS's can be locked together, thus allowing no drift between them.

Analog techniques do still have their advantages. Compared with a DDS, higher output frequencies are possible with an analog synthesizer. It is also has better spurious noise performance because its output is continuous and no quantization is involved, and a lower cost is entailed if the requirements are simple.

IMPLEMENTED DDS SYSTEM

The system implemented generally consists of a microcontroller subsystem and a DDS subsystem. (Figure 3) An additional power subsystem supplies the power and positive/negative voltage requirements of the two major subsystems. A PC serves as the user interface and sends the user choices through an RS-232 serial connection to the microcontroller subsystem.

Processing the data that comes from the PC, The microcontroller subsystem is responsible for sending the proper data and control signals to the DDS subsystem to obtain the desired output. It uses a 68HC11A1 8-bit microcontroller from Motorola and contains ROM, RAM and supporting reset, logic and address decoding circuitry.

The DDS subsystem (Figure 4) consists of a Qualcomm Q2334 dual DDS chip and a pair of digital-to-analog converter (DAC) and low-pass filter (LPF) combinations. The Q2334 is clocked at 50 MHz and uses a 32-bit phase accumulator. The DAC used is the 10-bit 100 M samples per second Q2510 also from Qualcomm while the LPF is a 7-pole elliptical type.

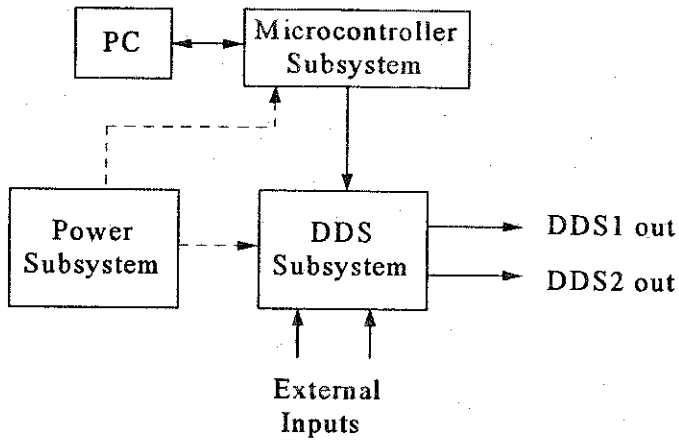

Figure 3. Block diagram of implemented DDS system

Data for modulating the DDS may come internally from the PC through the serial connection or may be externally-sourced. The external phase modulator processes and converts external signals into a form suitable for input to the external modulation pins of the Q2334.

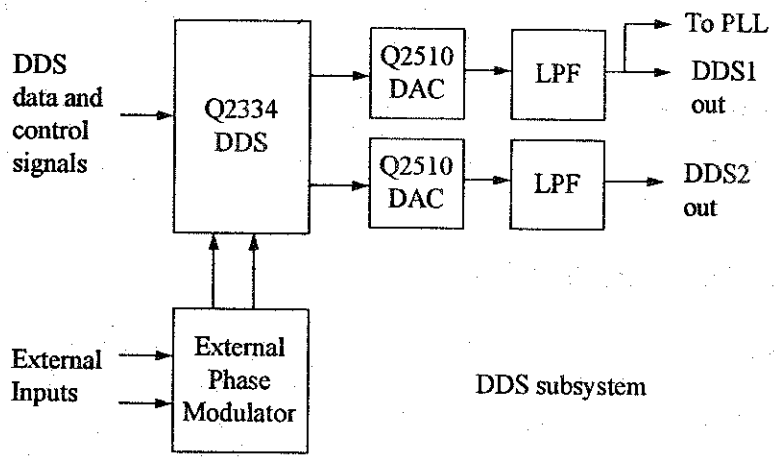

Figure 4. Black diagram of DDS subsystem

RESULTS OF IMPLEMENTED SYSTEM

Accordingly, with a 32 bit phase accumulator, the Q2334 should be able to achieve a frequency resolution of 50MHz / 2^{32} phase increments or 0.012 Hz per phase increment. This could not be verified, however, because no measurement equipment with a high enough resolution

was available. Pushing a digital scope to its limit however, a half-cycle can be shown (Figure 1) through which the DDS lower limit of 0.012 Hz can be approximately calculated. A 1 Hz sine wave is also shown in Figure 2.

The frequency accuracy of the DDS output was monitored using a Philips/Fluke PM6677 2.3 Ghz frequency counter. (Table 1) This counter has a 3 Hz lower limit, so readings start at 10 Hz.

Table I

Desired Frequency	DDS Output	Deviation (Hz)	Deviation (ppm)
10 Hz	10.0009 Hz	0.0009	89.99
100	99.9987	0.0013	13.00
1 Khz	999.9938	0.0062	6.20
10	9999.9753	0.0247	2.47
100	99.9998 Khz	0.2000	2.00
1 Mhz	999.9979	2.1	2.10
2	1999.9958	4.2	2.10
3	2999.9936	6.4	2.13
4	3999.9914	8.6	2.15
5	4999.9893	10.7	2.14
6	5999.9872	12.8	2.13
7	6999.9854	14.6	2.09
8	7999.9833	16.7	2.09
9	8999.9806	19.4	2.16
10	9999.9786	21.4	2.14
11	10999.9767	23.3	2.12
12	11999.9746	25.4	2.12
13	12999.9728	27.2	2.09
14	13999.9708	29.2	2.09
15	14999.9688	31.2	2.08
16	15999.9671	32.9	2.06
17	16999.9642	35.8	2.11
18	17999.9635	36.5	2.03
19	18999.9624	37.6	1.98
20	19999.9600	40.0	2.00

It is observed that starting from 10 Khz, all frequencies synthesized have deviations of less than 2.50 ppm. At lesser frequencies, this deviation increases but the fact is that the results are still very much acceptable. The standard acceptable level of frequency stability is at 100 ppm and the 89.99 ppm at 10 Hz is still within this limit. It is even a big possibility that this relatively large deviation at 10 Hz is due only to the measurement limitations of the frequency counter used. The DDS output is generally even better than that of a crystal oscillator which deviates to usually around 10 ppm.

The switching speed of the DDS is changing from one frequency to another in continuous wave (CW) mode was analyzed using an HP53310A Modulation Domain Analyzer. (Table 2) Listed below are the typical switching speeds (5 trials each) for frequency shifts from 1 MHz to 2 MHz and vice-versa, and from 7 MHz to 8 MHz and vice-versa.

Table 2

	1 MHz to 2 MHz (usec)	2 MHz to 1 MHz (usec)
Trial 1	6.600	7.367
2	6.400	4.467
3	6.500	6.200
4	6.000	6.700
5	7.333	6.767
Average	6.567	6.300

	7 MHz to 8 MHz (usec)	8 MHz to 7 Mhz (usec)
Trial 1	3.644	2.400
2	3.689	3.689
3	3.733	3.600
4	3.778	2.444
5	3.600	3.644
Average	3.689	3.155

Since the registers of the Q2334 DDS chip are double-buffered, values written into them do not take effect until the HOP CLK pin is pulsed or until any value is written into the AHC register. These time periods represent therefore the actual time it takes to switch from one frequency to another, exclusive of the time it takes to write the registers.

It is easily seen that relatively less time is taken when switching between high frequencies than when switching between lower frequencies. This is because comparatively, it takes less phase increments to complete a whole period for a higher frequency than for a lower frequency.

With a frequency stability of generally < 2.50 ppm and switching times of < 10 us, the DDS has proven itself to be superior baseband frequency synthesizer.

Figure 5 to 11 are typical spectrum and scope plots of the different synthesizing functions of the DDS board. Figures 7 and 8 show a BFSK output while Figure 9 is a frequency hopping

spectrum. The same 256 PSK output in frequency and time domains is shown in Figures 10 and 11.

The maximum data rate for external FSK and PSK modulation modes is 12.5 Mbaud per second. This data rate is determined by the minimum time needed before the external modulation pins MUXCLK or PMCLK of the Q2334 may be asserted again, which is 4 system clock periods. The maximum data rate for internal FSK and PSK modulation for this system is less than 4800 baud per second. This is because the modulating data originates from the PC and has to pass through the 9600 baud serial interface. With polling used that needs an acknowledgment from the 68HC11 before a byte of data is sent, the effective link becomes 4800 baud. Machine cycle times needed to process the modulating data reduce the baud rate to less than 4800.

CONCLUSION

Direct digital synthesizers provide a relatively low-cost flexible and stable alternative to analog frequency synthesis. With its fine frequency resolution, fast switching speed and facility for m-ary digital modulation, it finds application in many important communication systems such as frequency hopping spread spectrum systems and digital microwave links. Many other commercial applications abound and it is but a matter of time before direct digital synthesis becomes a mature technology.

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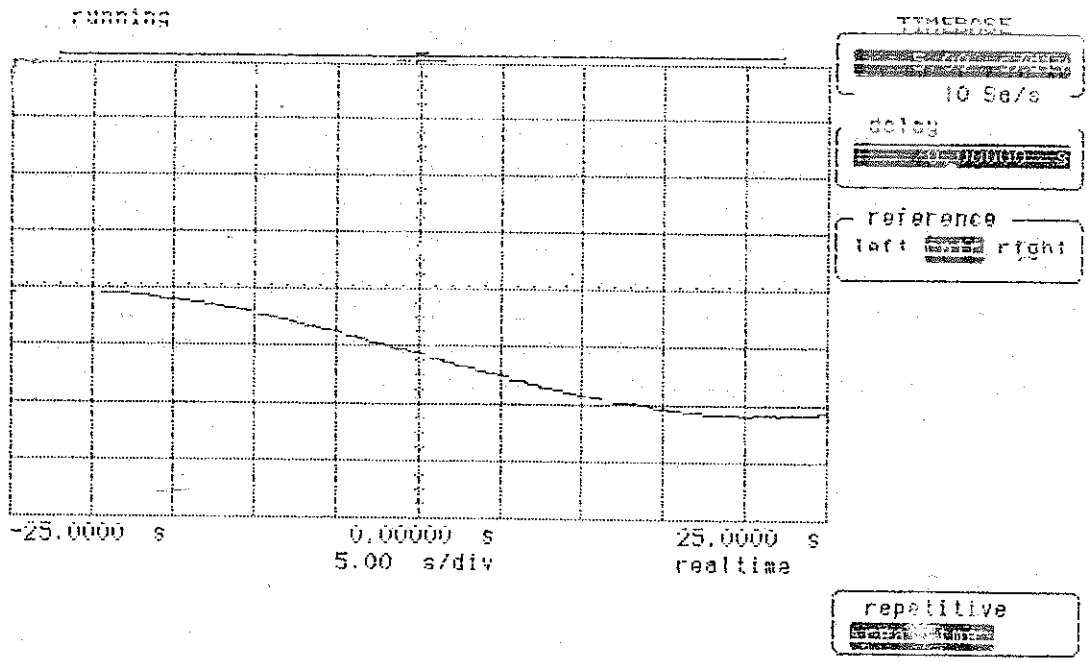

Figure 5. 0.012 Hz DDS output (half-cycle)

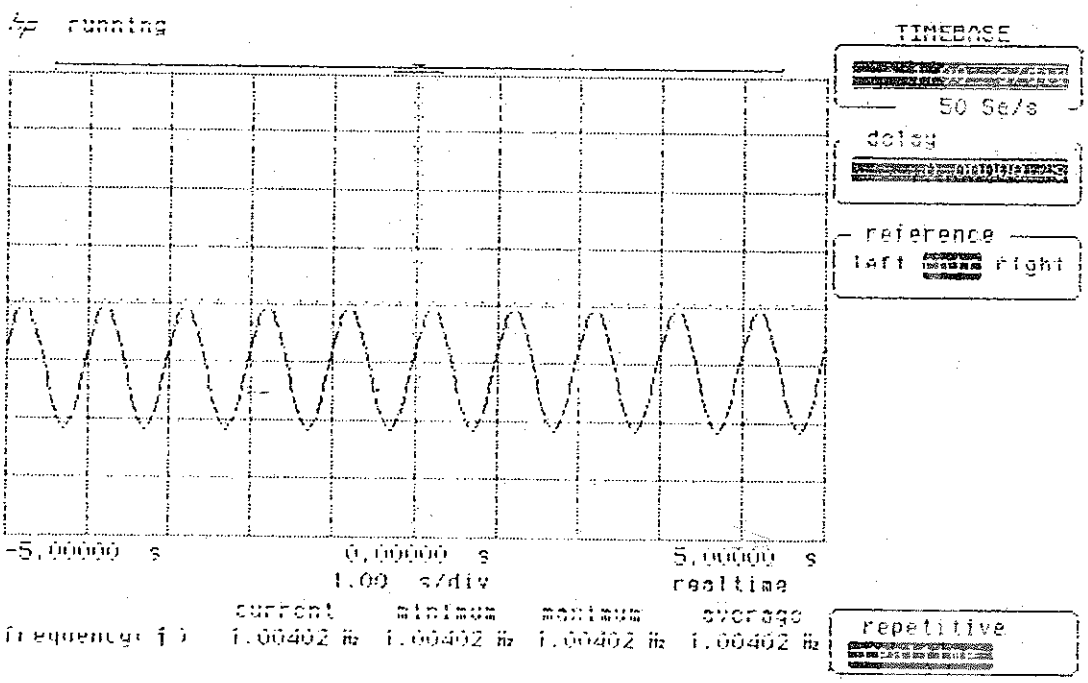

Figure 6. 1 Hz DDS output

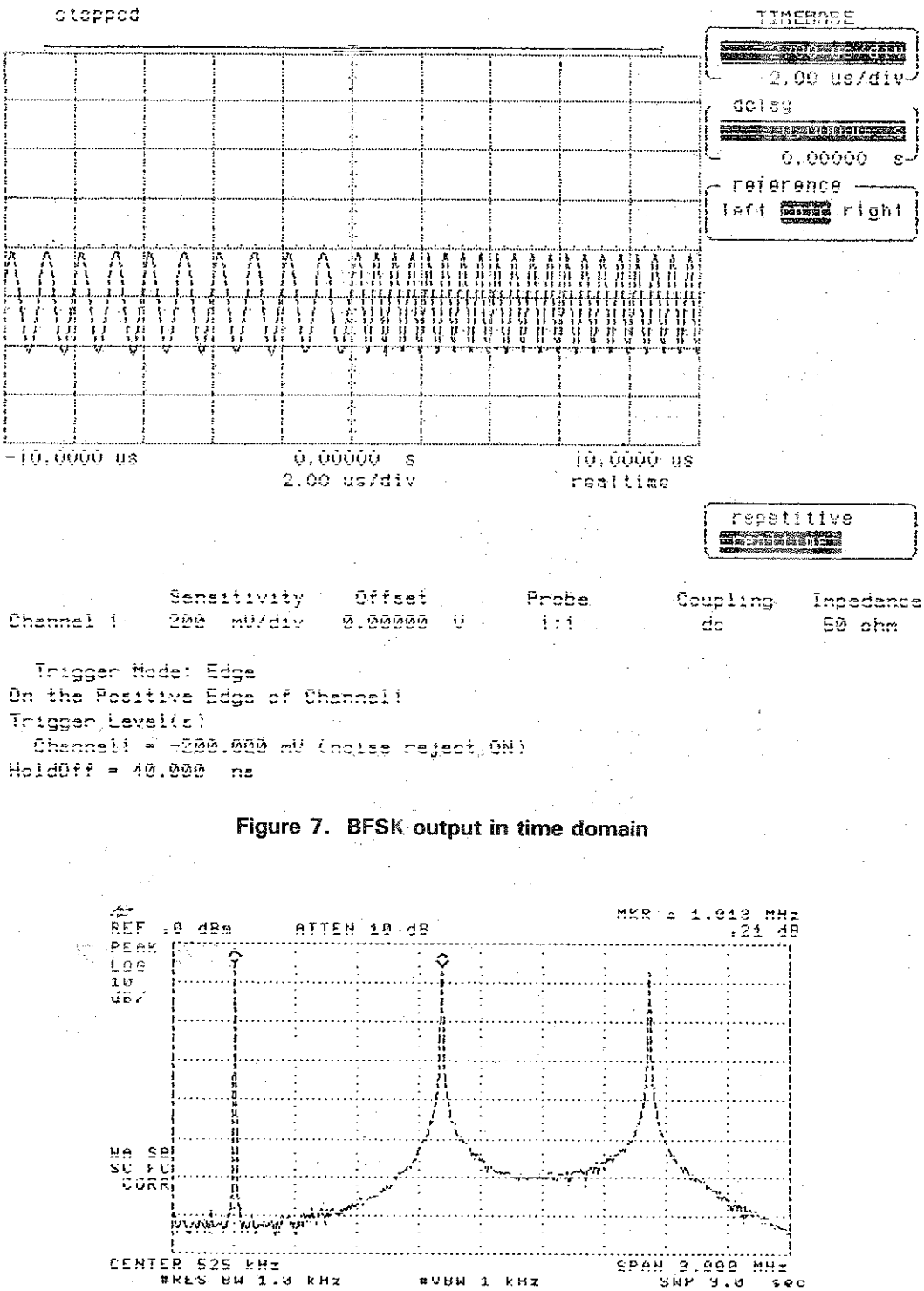

Figure 7. BFSK output in time domain

Figure 8. BFSK output spectrum

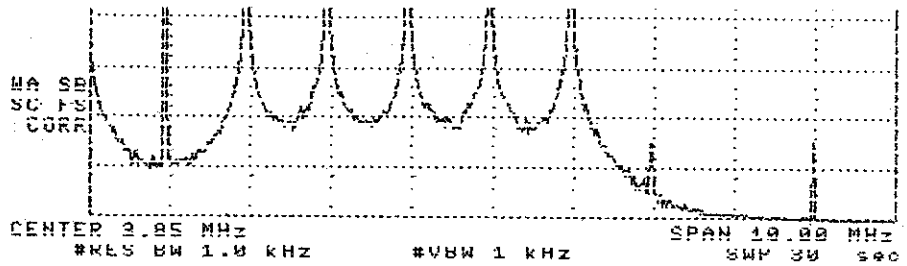

Figure 9. Frequency hopping

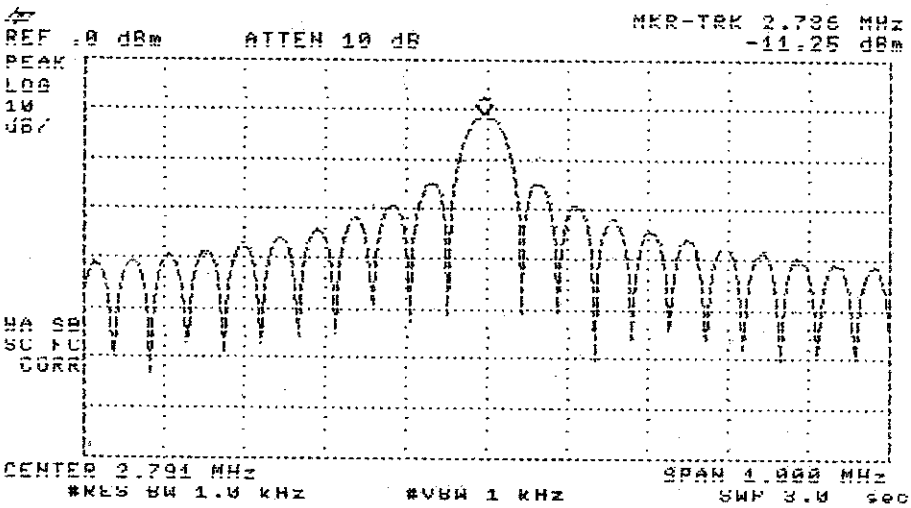

Figure 10. 256PSK output spectrum

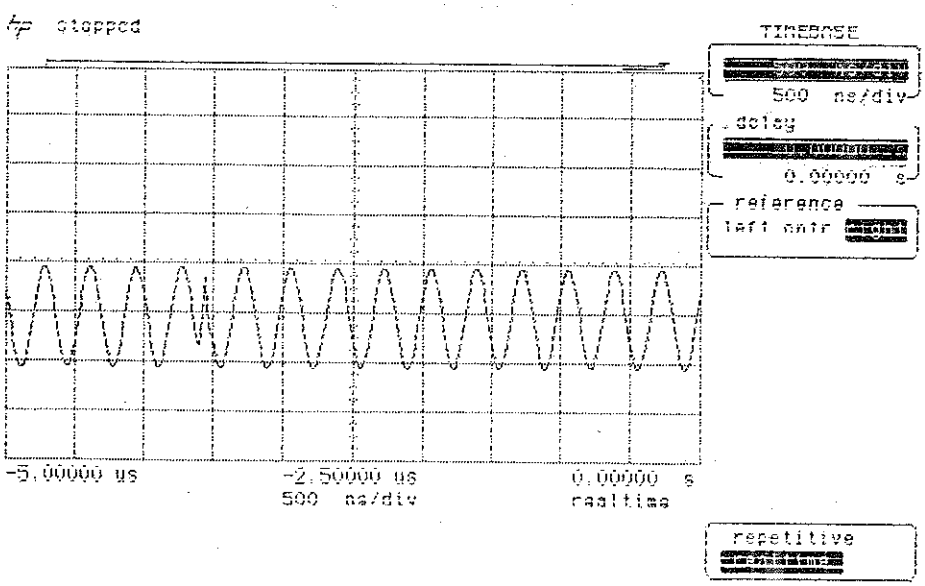

Figure 11. 256PSK output in time domain