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A TUTORIAL FOR ELECTRONIC CIRCUIT DESIGN USING SPICE

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ABSTRACT

A general approach to electronic circuit design is outlined. The iterative design path is identified to cite, particularly, the usefulness and the advantages of circuit simulation. Finally, a design example for a high voltage DC power supply is developed. Applying Spice demonstrates the usefulness of circuit simulation in the iterative process of circuit design before the circuit is built and after one thinks the design is complete.

Author's Note: The paper assumes some familiarity with Spice and a background in engineering electronics.

INTRODUCTION

Computers during the last 30 years have become part of the engineers design toolset. Computers have the power to contribute "better enabling" of ones efforts in the tedious process of design.

SPICE (Simulation Program with Integrated Circuit Emphasis) has numerous uses. Its main use is in analog simulation electronic circuit responses to test stimuli especially for integrated circuits. Extensions of the original command set of Spice has allowed other uses like Analog Behavioral modeling and combine Digital-Analog Simulation.

This paper shall explore some possible benefits of using Spice in the iterative process of discrete circuit and system design which should lessen design turn around time, increase the designer's proficiency and confidence, promote circuit refinements and circuit performance.

AN APPROACH TO ELECTRONIC DESIGN

an approach to electronic design. As usual, design starts out with an idea, be it for a new product (product development) or for a new application (application development). The development). The idea may originate from the designer himself, the user end, or a client who sees nice opportunities in the consumer market.

Product behavioral requirements are laid down which are then translated to technical specifications of the overall system by the designer. Acceptance criteria are then established. Next a rough skecth of the functional block diagrams for several trial systems are laid out. Each proposed block level diagram is examined at the system level for its technical operability and inter operability.

Next, circuit details and component values are selected then analyzed for proper operation. Errors are then spotted and corrected. The circuits are then constructed, tested, and debugged for conformance to specifications. Finally, the delivery is made to the end user.

In the design process, the electronics design engineer attempts to minimize design time, refine/simplify the circuit, improve circuit performance. Spice helps you do this *before* you build the circuit. This lets you decide if changes are needed, without touching any hardware. Also, simulation allows you to check your design *after* you think it is complete. This improves the chances of a successful design and helps spot weakness in the design that may lead to probable failure. Moreover, circuit refinements can lead to high performance, reliable operation under service conditions and good yield.

WHY SIMULATE WHEN YOU CAN BUILD ?

Typically your designs are pressed for schedule time, budget expense, and manufacturing yield. With a simulation program you can

1)Reduce design lead time by

- checking a circuit idea before building a prototype, even before buying or waiting for parts (forward engineering)
- quickly revise a design , making many versions of it
- hasten the understanding and checking the details of circuit operation of a published design, adapting revisions and verifying them in a short span of time (reverse engineering)

2)determine design performance and possible improvemnets by

- by determining the key (sensitive) parameters in a design
- refining or improving an existing design
- developing library circuits of proven designs that are integratable with new , prototype designs
- driving subsections of a design to identify and isolate limiting effects in your design

- making simulated test measurements which are difficult (due to electrical noise or circuit loading), inconvenient (lack of special test equipement) or unwise (the test circuit would destroy itself)

- simulating a circuit many times with component variations to check what percentage will pass "final test" and which combinations give the "worst case" results.

To know what to expect out of a design (performance, dependability, conformance to specifications [quality], variability) allows a designer to commit it for fabrication at the earliest possible time and perhaps inculcate refinements that make it robust, attain a "tighter spec" or even make it less expensive to produce.

ADDING SPICE TO YOUR TOOLBOX

Like any new tool, experience is required to get the most benefit from it. A successful use as described requires some background preparation.

Spice assumes you are able to operate the computer that will run the simulator as well as create the input for the simulator.

A more important aspect however is that designers must be reoriented. "Back to the basics" should be a thrust of this reorientation.

Spice assumes that you have a passing acquaintance with electronic circuits (series, parallel, cascaded and feedback circuits,), passive component (resistors, capacitors , inductors), active components (bjt,jfet, mosfet, independent and controlled sources), and network analysis (Ohms, KVL, KCL laws, complex numbers, impedance functions, admittance functions, etc.)

Extending the use of Spice to other non-electrical systems "by analogy" requires the broader understanding of linear system theories.

Modelling limitations must be understood. Model limitations lead to devices that don't "blow up" in the simulation runs. It's up for the designer to watch out for the device stresses due to voltage, current, and power levels. You have to look at the results to see if they make sense in your application.

It leaves the design problem up to the designer. It does not make designs for you. It will not tell you that your circuit needs compensation or will hint that there is a better circuit or that a section needs a clipping circuit.

Instead it is dumb enough not to know, how you expect your circuit to work, thus it arrives at response calculations independently of your expectations on circuit operation. Spice makes no assumptions on how the circuit should behave. As long as Spice is able to solve your circuit matrix, it will do so.

GETTING STARTED

Begin with a quick circuit to introduce yourself to running SPICE. This will show you the basics of circuit simulation without getting complicated by rules, details, exceptions and so on, and quickly get to a successful result.

Later extend to the wide range of features and ways of combining these to express complex circuit functions.

The following example is simple. The design process is demonstrated step by step. The problem is to design a high voltage DC power supply at 200 Vdc for a load current of 0 to 100 ma. The load regulation should be 1% or better.

Figure 2a shows the basic linear series pass transistor element that connects the 300 volt unregulated DC to the load.

The SPICE input file is:

```
* High Voltage Power Supply
* Figure 2: Basic Series Pass Element
Vcc      1     0            DC    300
Rbase    1     2                  20K
Rload    3     0                  1Meg
Qpass    1     2     3            QMine
Icont    2     0            DC    10ma
Iload    3     0            DC    100ma
.dc lin iload      0     .2     .02
+      lin icont      0     .01     1.000m   ; .MODEL qmine  NPN(IS = 974.4E-15 XTI = 3
EG = 1.11 VAF = 450  +  BF = 40.0 NE = 1.941 ISE = 902.5E-12 IKF = 4.029 XTB = 1.5  +
BR = 2.949 NC = 2 ISC = 0 IKR = 0 RC = .1 CJC = 276.1E-12 VJC = .75  +  MJC = .3333 FC = .5
CJE = 569.1E-12 VJE = .75 MJE = .3333  +  TR = 971.7E-9 TF = 39.11E-9 ITF = 20 VTF = 10
XTF = 2)
.end
```

Figure 2b shows the results of the run. The control current is stepped from 0 to 10ma with a 1ma. increment. For a given control current, the output voltage drops as the load current increases. To keep the output at 200 volts, the control current is 5ma. when Iload = 0 and is about 2.5ma when Iload = 100ma. This can be handled by a small power transistor with high gain.

In Figure 3a, the control current has been replaced with a control transistor, (the error amplifier), and zener diode reference. Now a control voltage feeds the base of the error amplifier.

The Spice Input File is:

```
* High Voltage Power Supply
* Figure 3: Error amplifier and zener reference added
Vcc      1      0      DC    300
Rbase    1      2            20K
Rload    3      0            1Meg
Rdd      4      0            33K
Rberr    6      4            4.7K
Qpass    1      2     .3     Qpower
Qerr     2      4      5     Qsmall
Dzener   0      5            D1N4749
Vlcont   6      0      DC    25
Iload    3      0      DC    100ma
.dc lin vicont      0      30      1
+      lin iload      0      .2      .5      ;
.MODEL qpower  NPN(IS=974.4E-15 XTI=3 EG=1.11 VAF=450 + BF=40.0 NE=1.941
ISE=902.5E-12 IKF=4.029 XTB=1.5    + BR=2.949 NC=2 ISC=0 IKR=0 RC=.1
CJC=276.1E-12 + VJC=.75 MJC=.3333 FC=.5 CJE=569.1E-12 VJE=.75
+ MJE=.3333 TR=971.7E-9 TF=39.11E-9 ITF=20 VTF=10 TF=2)
.MODEL qsmall  NPN(IS=974.4E-15 XTI=3 EG=1.11 VAF=450
+ BF=140.0 NE=1.941 ISE=902.5E-12 IKF=4.029 XTB=1.5 + BR=2.949 NC=2 ISC=0
IKR=0 RC=.1  CJC=276.1E-12 + VJC=.75 MJC=.3333 FC=.5 CJE=569.1E-12 VJE=.75
+ MJE=.3333 TR=971.7E-9 TF=39.11E-9 ITF=20 VTF=10 TF=2)
.lib c:\pspice\lib\diode.lib
.lib c:\pspice\lib\bipolar.lib
.end
```

Figure 3b shows the run result: a typical transfer curve with inversion. The curves indicate that the useful control range is non-linear but with a steep slope(high gain, about 190 times) within the control voltage range 28 to 30 volts. Thus in closed loop, the control voltage should stay in this range if regulation is to be maintained. A higher gain is possible if the 4.7K base resistance is removed. This brings the control voltage down to the 20 to 25 volt range.

In order to preserve the gain, a fet is added to provide medium impedance drive required by the error amplifier. At the same time, its high input impedance minimizes loading at the feedback tap connection, thus preserving the feedback return ratio.

Figure 4a shows the additions. A zener clamp is used so that low voltages fets may be employed.

The Spice input file is:

```
* High Voltage Power Supply
* Spice Input file for Figure 4: Fet Added, Open loop

Vcc      1    0     DC   300
Rbase    1    2          20K
Rload    3    0          1Meg
Rdd      4    0          33K
rd       1    6          100k
rgs      7    0          100k
Qpass    1    2     3    Qpower
Qerr     2    4     5    Qsmall
Jfet     6    7     4    Jfet
Dref     0    5          D1N4749
Dzener   0    6          Dzener
Vlcont   7    0     DC   25
Iload    3    0     DC   100ma
.dc lin vicont    0    25    1
+ lin iload       0    .2    .1    ;
.MODEL qpower  NPN(IS=974.4E-15 XTI=3 EG=1.11 VAF=450 + BF=40.0 NE=1.941
ISE=902.5E-12 IKF=4.029 XTB=1.5 + BR=2.949 NC=2 ISC=0 IKR=0 RC=.1
CJC=276.1E-12 VJC=.75 + MJC=.3333 FC=.5 CJE=569.1E-12 VJE=.75 MJE=.3333
+ TR=971.7E-9 TF=39.11E-9 ITF=20 VTF=10 XTF=2)
.MODEL qsmall  NPN(IS=974.4E-15 XTI=3 EG=1.11 VAF=450 + BF=140.0 NE=1.941
ISE=902.5E-12 IKF=4.029 XTB=1.5 + BR=2.949 NC=2 ISC=0 IKR=0 RC=.1
CJC=276.1E-12 + VJC=.75 MJC=.3333 FC=.5 CJE=569.1E-12 VJE=.75
+ MJE=.3333 TR=971.7E-9 TF=39.11E-9 ITF=20 VTF=10 TF=2)
*
.model Jfet   NJF(Beta=1.304m Betatce=-.5 Rd=1 Rs=1 + Lambda=2.25m Vto=-3
Vtotc=-2.5m Is=33.57f Isr=322.4f + N=1 Nr=2 Xti=3 Alpha=311.7 Vk=243.6
Cgd=1.6p M=.3622 + Pb=1 Fc=.5 Cgs=2.414p Kf=9.882E-18 Af=1)
*
.MODEL Dref   D(IS=0.05UA RS=15 BV=24.00 IBV=0.05UA)
*
.MODEL Dzener   D(IS=0.05UA RS=15 BV=30.0 IBV=0.05UA)
.lib c:\pspice\lib\diode.lib
.lib c:\pspice\lib\bipolar.lib
.end
```

Figure 4b show open loop results. The load current is stepped in 100ma increments from 0 to 200ma. The diagonal lines bound the area of interest and thus indicates the return ratio (feedback factor, Beta). A feedback factor (Beta) of 1/10 yields a high output voltage. A feedback factor of 1/6 yields a low output voltage. A feedback of 1/9 seems to be just right. Regulation can also be estimated from the intersections of the diagonals with the different load currents.

Finally the loop is closed with the feedback factor selected as 1/9. This is formed by the ratio divider.

Beta = Rgs/(Rgs + Rgg)
with Rgg selected as about 800.5k
Rgs as 100K

The Spice file is:

```
* High Voltage Power Supply
* Spice Input file for Figure 5: Vfb Closed loop
Vcc       1    0    DC   300
Rbase     1    2         20K
Rload 3   0         1Meg
Rdd       4    0         33K
rd        1    6         100k
rgg       3    7         800.5k
rgs       7    0         100k
Qpass     1    2    3    Qpower
Qerr      2    4    5    Qsmall
Jfet      6    7    4    Jfet
Dref      0    5         D1N4749
Dzener    0    6         Dzener
Iload 3   0    DC   100ma
.dc lin iload0.2.5;
.MODEL qpower NPN(IS=974.4e-15 XTI=3 EG=1.11 VAF=450 +
BF=40.0 NE=1.941 ISE=902.5E-12 IKF=4.029 XTB=1.5 + BR=2.949
NC=2 ISC=0 IKR=0 RC=.1 CJC=276.1E-12 VJC=.75 + MJC=.3333
FC=.5 CJE=569.1E-12 VJE=.75 MJE=.3333 + TR=971.7E-9
TF=39.11E-9 ITF=20 VTF=10 XTF=2)
.MODEL qsmall NPN(IS=974.4E-15 XTI=3 EG=1.11 VAF=450 +
BF=140.0 NE=1.941 ISE=902.5E-12 IKF=4.029 XTB=15 +
BR=2.949 NC=2 ISC=0 IKR=0 RC=.1 CJC=276.1E-12 VJC=.75 +
MJC=.3333 FC=.5 CJE=569.1E-12 VJE=.75 MJE=.3333 +
TR=971.7E-9 TF=39.11E-9 ITF=20 VTF=10 XTF=2)

.model Jfet NJF(Beta=1.304m Betatce=.5 Rd=1 Rs=1 +
Lambda=2.25m Vto=-3 Vtotc=2.5m Is=33.57f Isr=322.4f + N=1 Nr=2 Xti=3
Alpha=311.7 Vk=243.6 Cgd=1.6p M=3622 + Pb=1 Fc=.5
Cgs=2.414p Kf=9.882E=18 Af=1)
.MODEL Dref D(IS=0.O5UA RS=15 BV=24.00 IBV=0.05UA)

.MODEL Dzener D(IS=0.05UA RS=15 BV=30.0 IBV=0.05UA)
.lib c:\pspice\lib\diode.lib
.lib c:\pspice\lib\bipolar.lib
.end
```

The output V v.s. I performance in figure 5 shows that the power supply meets the regulation requirements set forth.

Figure 6 indicates the semiconductor device ratings for sizing the components. Thus the zener reference diode can be a 1 watt unit, the zener clamp can be a 0.5 watt unit, the error amplifier and fet can be 300mW unit, and finally the pass transistor can be a 100 W unit. The 20K ohm is rated 20 watts.

Figure 7 indicates the efficiency of the power supply. The best efficiency is around 60% at full load.

CONCLUSION

Spice will contribute to better "enabling of ones efforts" in the tedious process of design but does not replace design experience. It relieves the setting up the equations and math grinding thus helping you to arrive a your prototype circuit design more quickly, more surely.

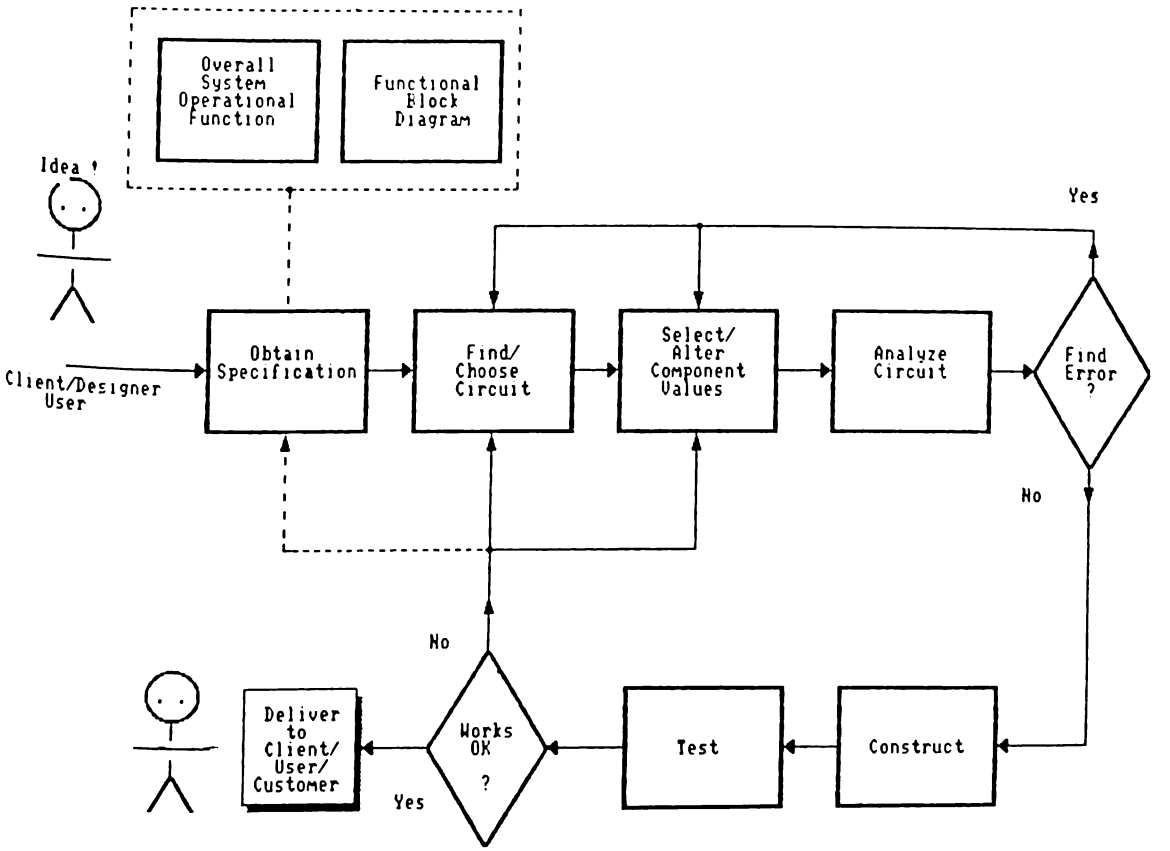
For the design's ultimate worth of course, the design must be built and tested in the final event, with real components, to fully close into the real thing the user can use.

REFERENCES

1. **Paul W. Tuinenga.** *Spice A Guide to Circuit Simulation & Analysis Using Pspice, MicroSim Corporation Prentice Hall c1988*

2. **Darold Wobschall.** *Circuit Design for Electronic Instrumentation, McGraw-Hill c1987*

3. **RCA,** *Power Transistor Applications*



An Approach to Electronic Design

Figure 1

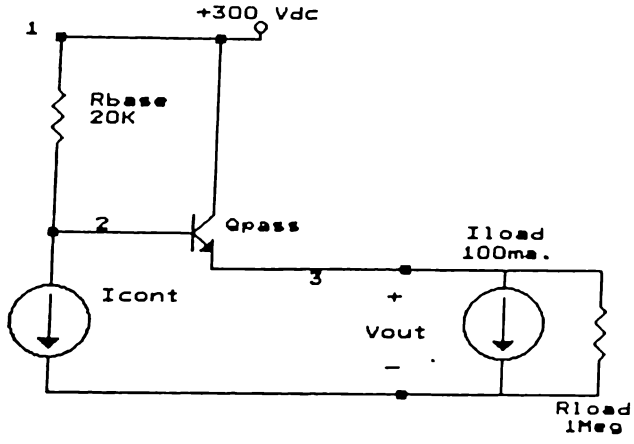


Figure 2a. Basic Series Pass Regulator

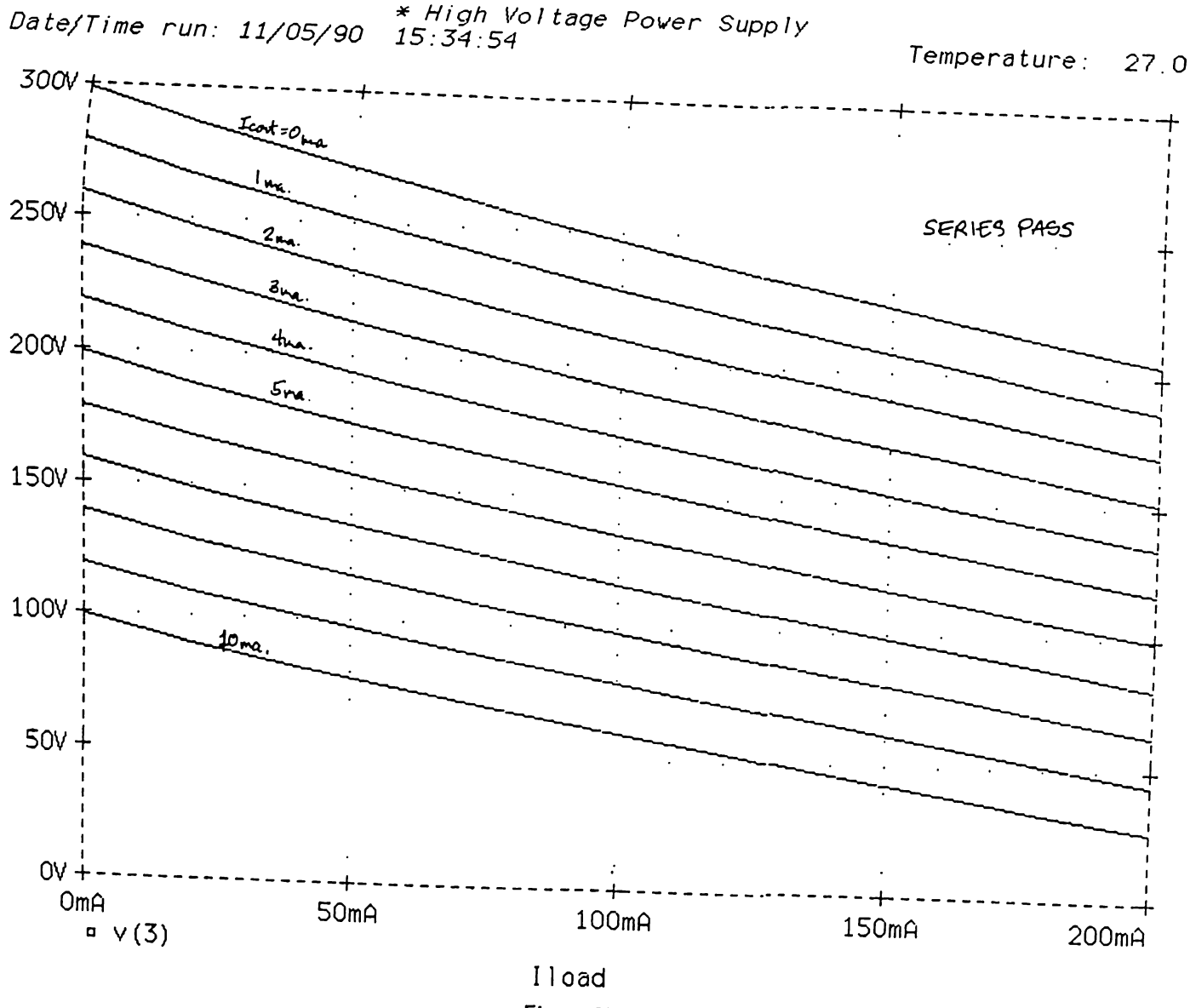

Date/Time run: 11/05/90
* High Voltage Power Supply
15:34:54
Temperature: 27.0
300V
250V
200V
150V
100V
50V
0V
Icont=0ma
1ma.
2ma.
3ma.
4ma.
5ma.
10ma.
SERIES PASS
0mA
50mA
100mA
150mA
200mA
V(3)
Iload

Figure 2b

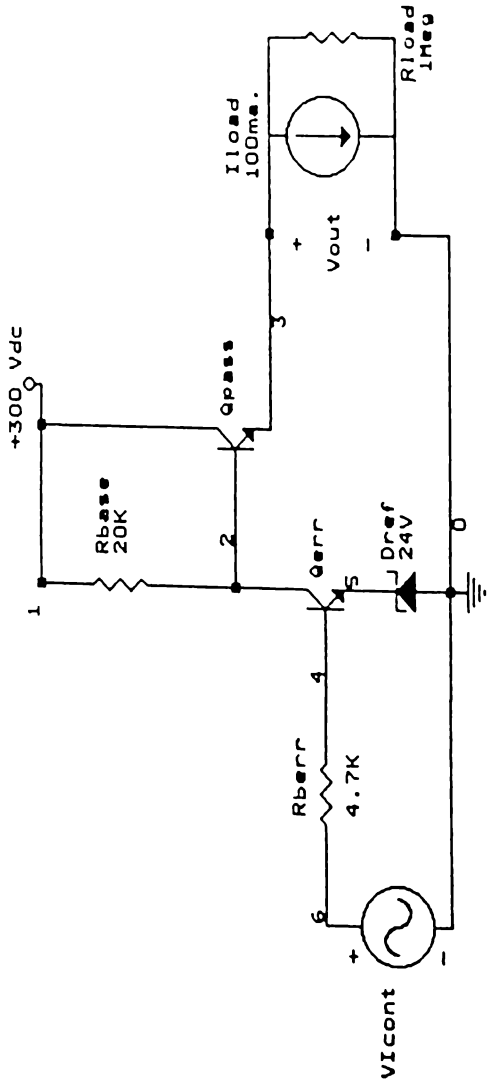


Figure 3a. Error control and Reference diode Added

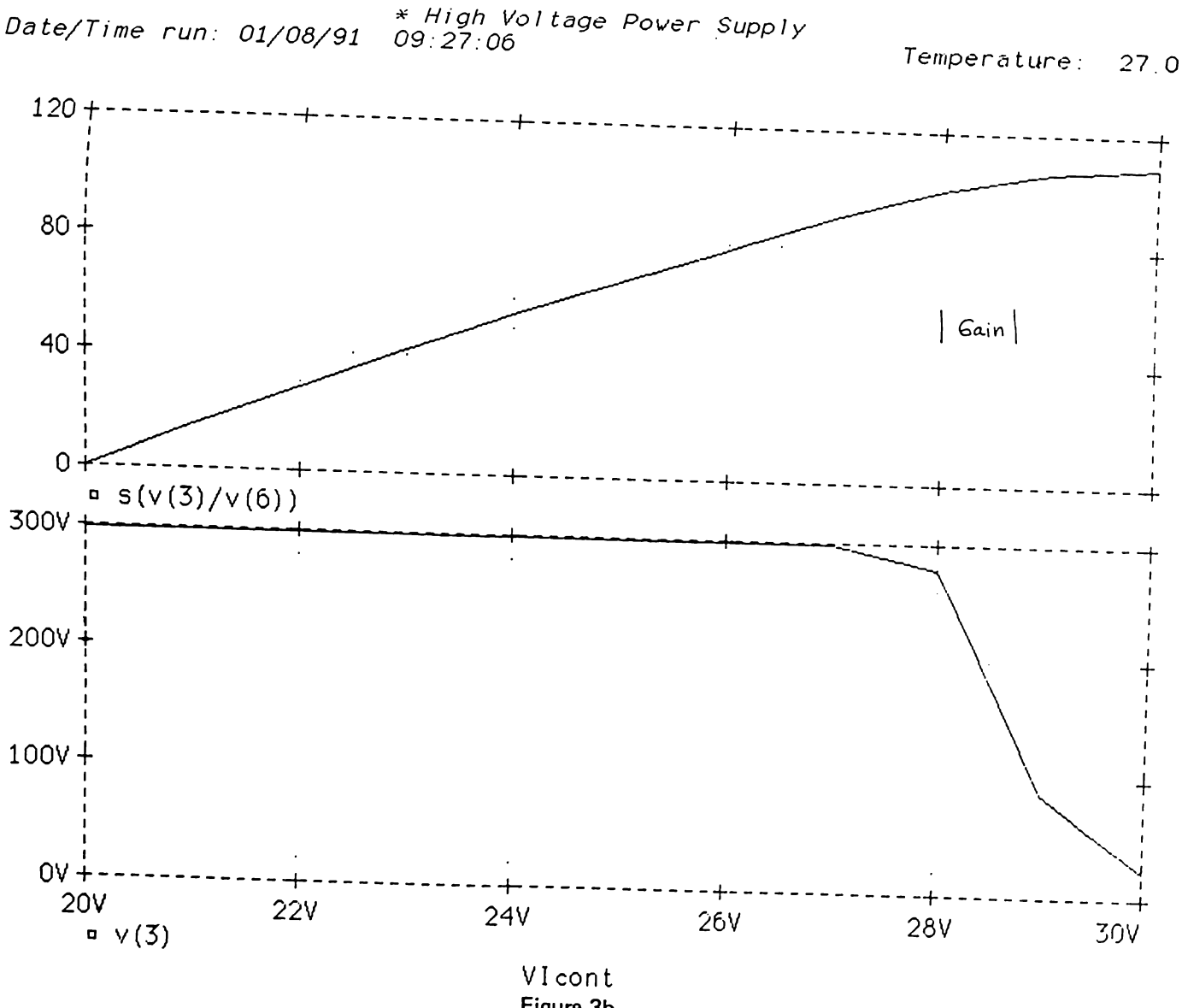

Date/Time run: 01/08/91 09:27:06
* High Voltage Power Supply
Temperature: 27.0
120
80
40
0
Gain
s(v(3)/v(6))
300V
200V
100V
0V
20V
22V
24V
26V
28V
30V
v(3)
VIcont

Figure 3b

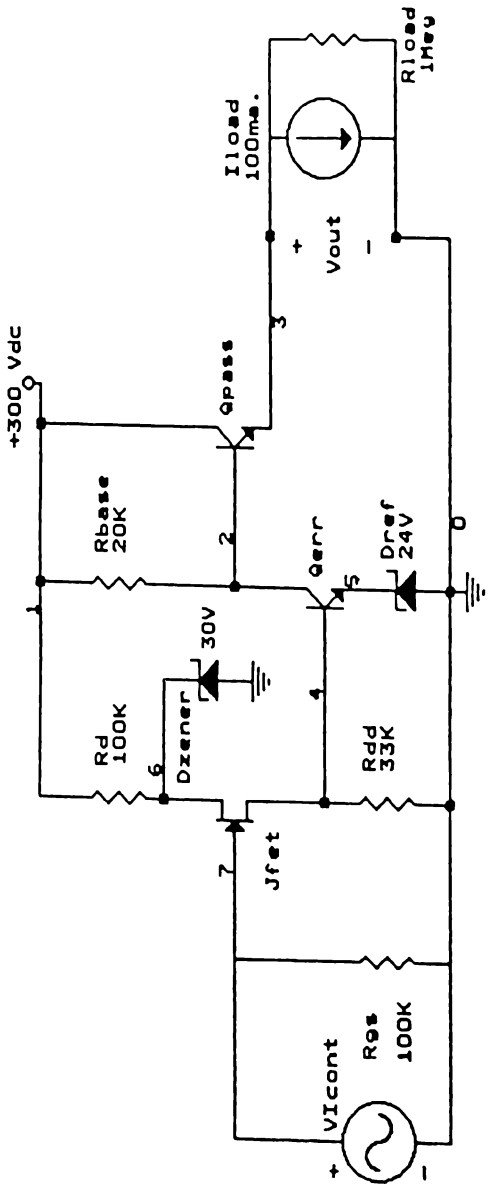


Figure 4a. Fet added for drive impedance match and high impedance isolation
Open Loop Analysis

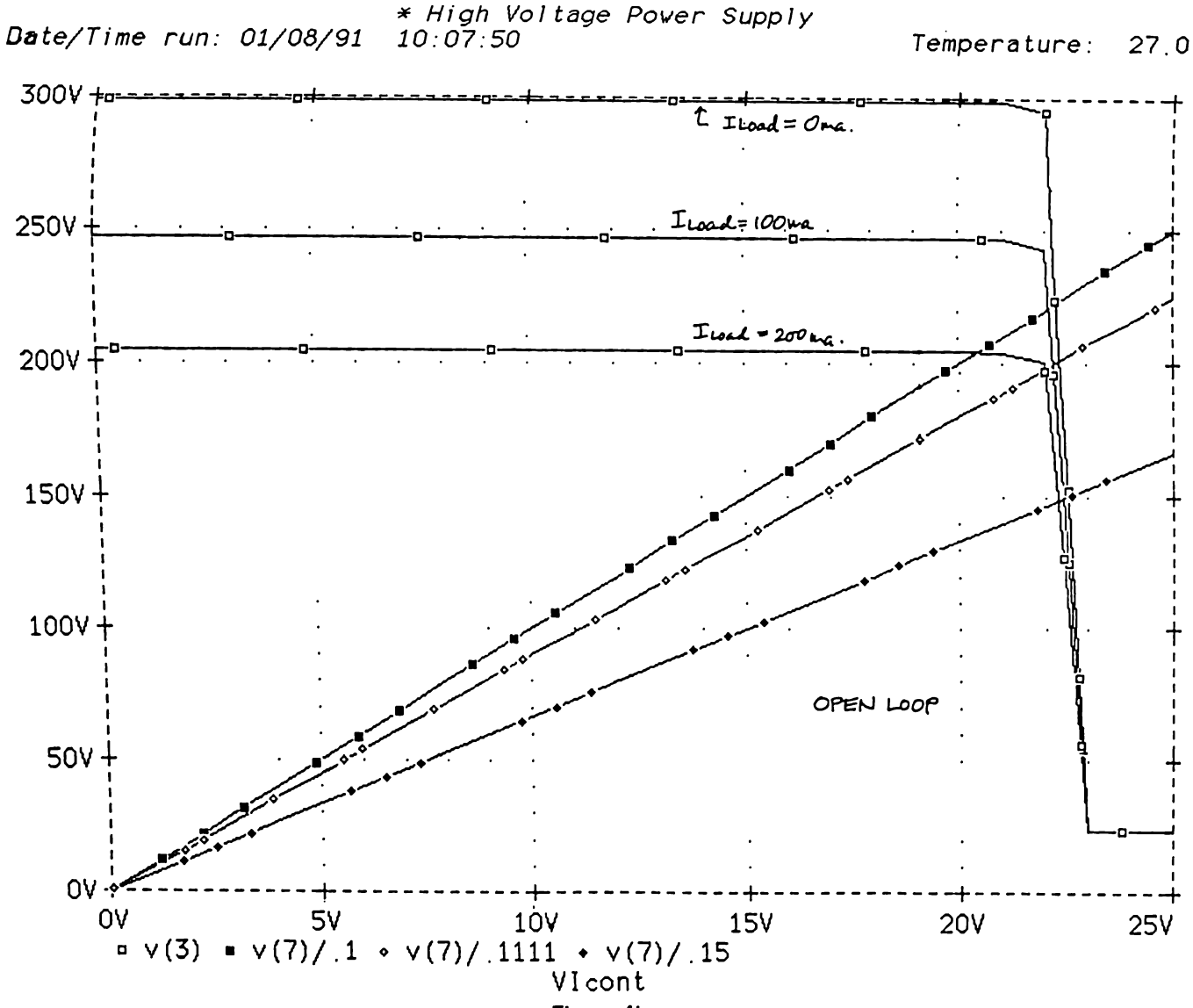

* High Voltage Power Supply
Date/Time run: 01/08/91 10:07:50
Temperature: 27.0
300V
250V
200V
150V
100V
50V
0V
0V
5V
10V
15V
20V
25V
ILoad = 0ma.
ILoad = 100ma
ILoad = 200ma.
OPEN LOOP
v(3) v(7)/.1 v(7)/.1111 v(7)/.15
VIcont

Figure 4b

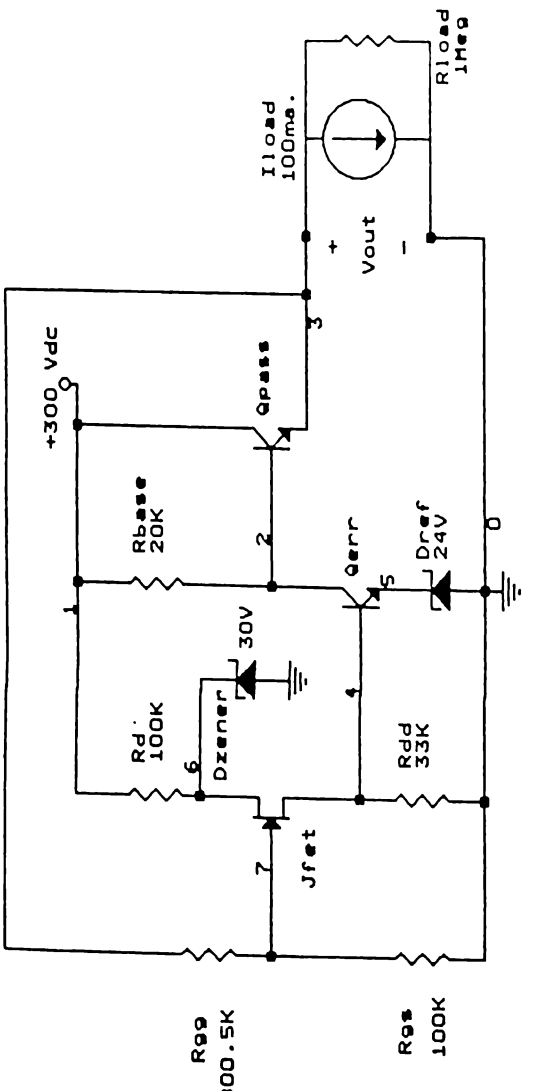


Figure 5a. Complete Final Schematic of 200 Vdc. 100 ma.
High Voltage DC Power Supply
Closed Loop Analysis

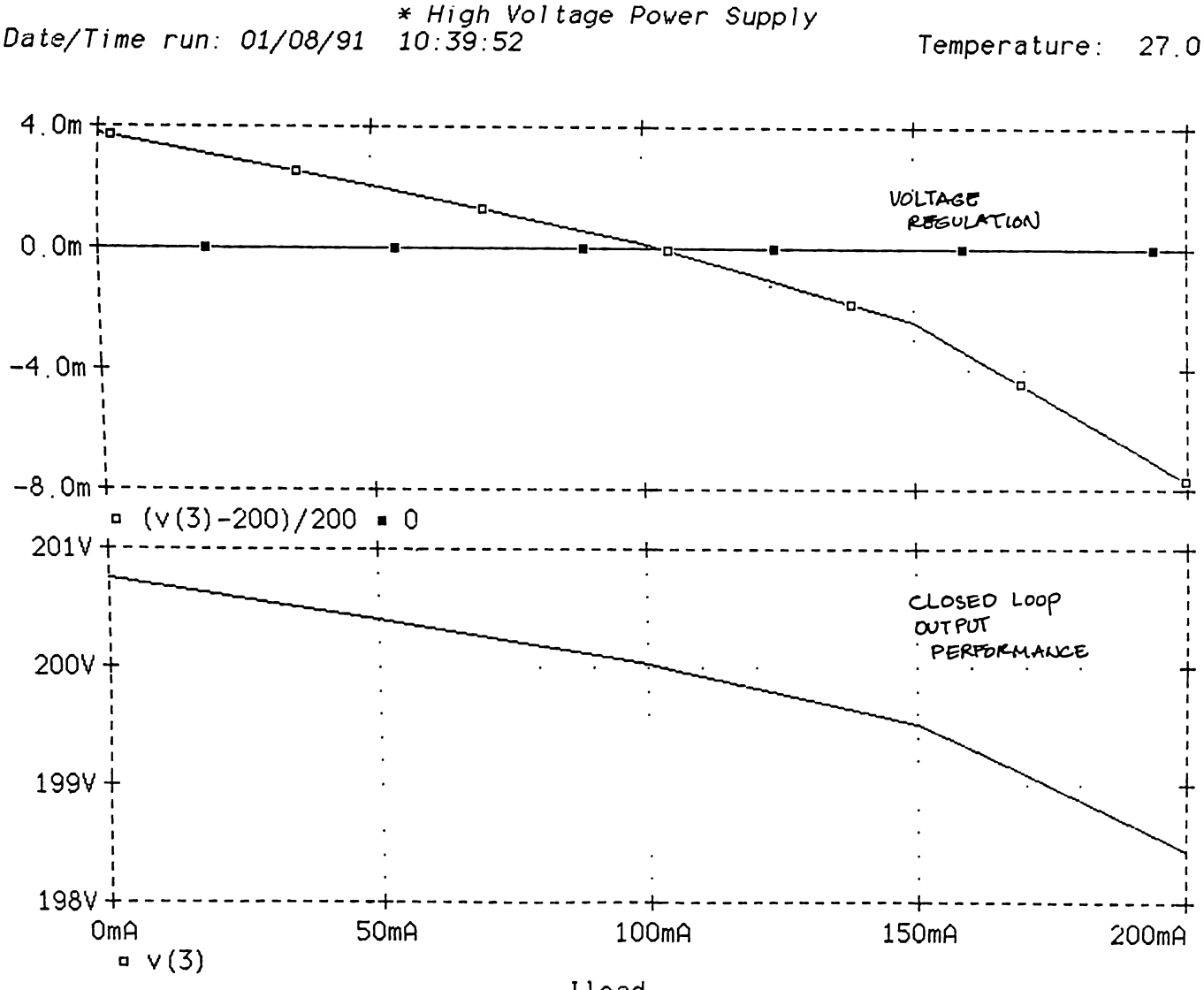

* High Voltage Power Supply
Date/Time run: 01/08/91 10:39:52
Temperature: 27.0
4.0m
0.0m
-4.0m
-8.0m
VOLTAGE REGULATION
(v(3)-200)/200
0
201V
200V
199V
198V
CLOSED LOOP OUTPUT PERFORMANCE
0mA
50mA
100mA
150mA
200mA
v(3)
Iload

Figure 5b

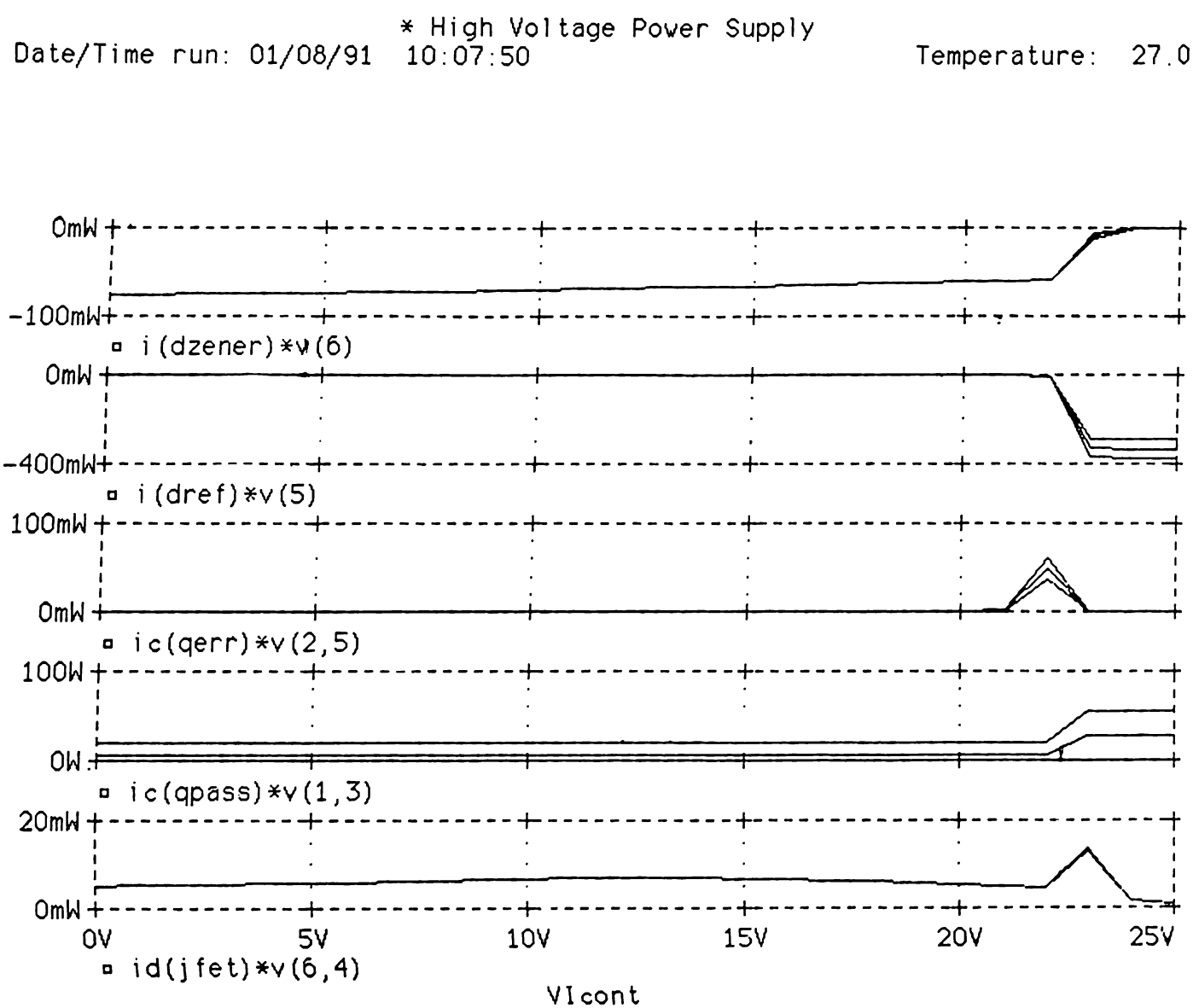

* High Voltage Power Supply
Date/Time run: 01/08/91 10:07:50
Temperature: 27.0
0mW
-100mW
i(dzener)*v(6)
0mW
-400mW
i(dref)*v(5)
100mW
0mW
ic(qerr)*v(2,5)
100W
0W
ic(qpass)*v(1,3)
20mW
0mW
0V
5V
10V
15V
20V
25V
id(jfet)*v(6,4)
VIcont

Figure 6

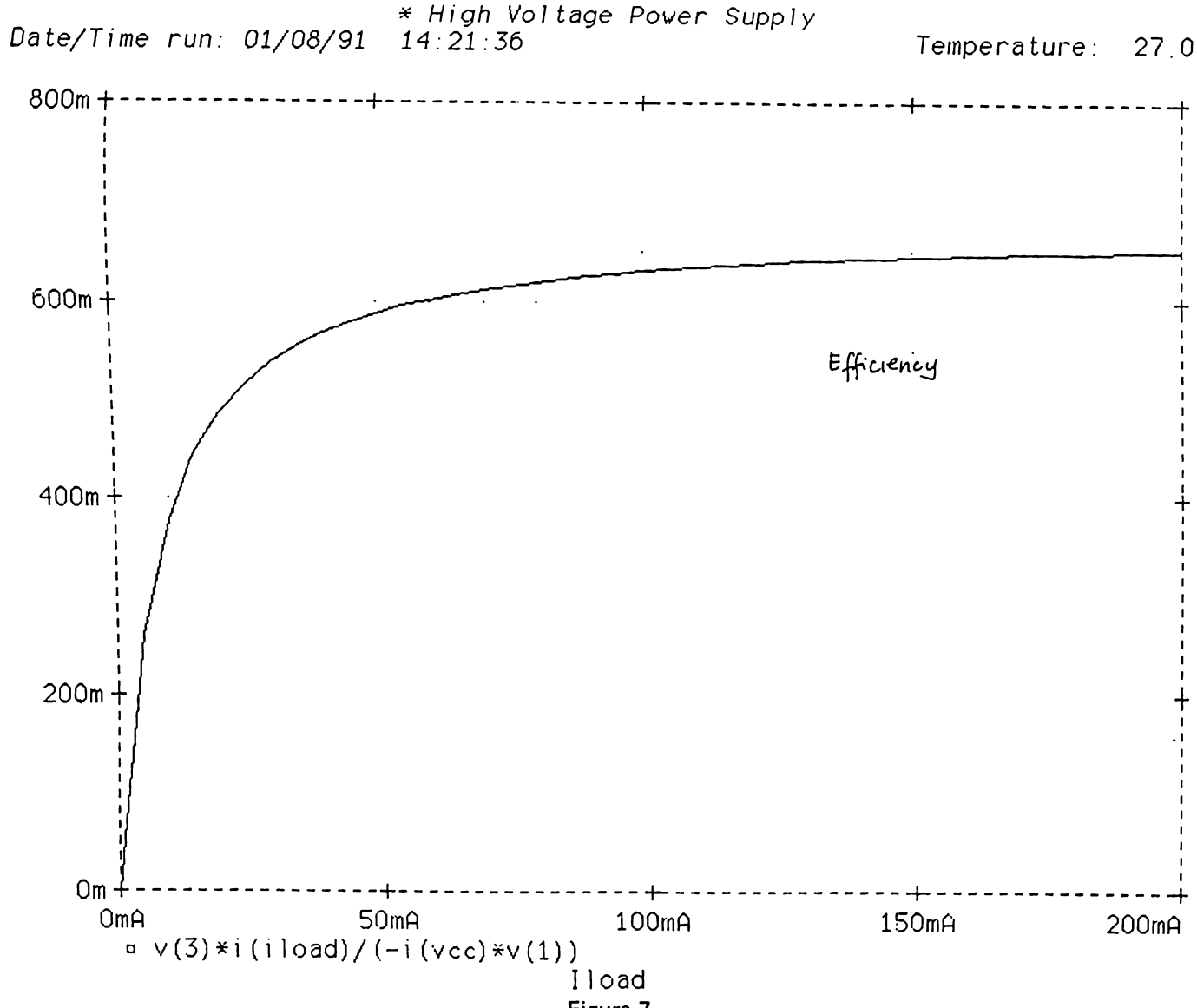

* High Voltage Power Supply
Date/Time run: 01/08/91 14:21:36
Temperature: 27.0
800m
600m
400m
200m
0m
Efficiency
0mA
50mA
100mA
150mA
200mA
v(3)*i(iload)/(-i(vcc)*v(1))
Iload

Figure 7