"it is convenient to analyze a differential amplifier using this particular model . . ."

On Teaching Different Amplifiers Using a "T" Transistor Model

by

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Abstract

This paper presents a practical circuit approach in the analysis of an emitter-coupled differential amplifier pair. Development and analysis center around parameter keywords like differential gain (AD), common mode gain (AC) and common mode rejection ratio (CMRR).The Ebers-Moll Model is used to derive a "T" transistor model for signal analysis.

Introduction

The differential amplifier forms an essential gain stage in today's operational amplifiers. Its ability to amplify and separate minute signals riding on large baseline potentials is made possible by virtue of its differential mode and common mode rejecting ratio (CMRR). This means that the output depends only on the difference between the input voltages and is not dependent in the magnitude of either input voltage. Thus interferring noise like 60 HZ hum is effectively rejected, electro-cautery potentials superimposed on ECG monitor signals are suppressed. The amplifier can perform down to direct current while retaining drift free performance. High gains are achieved by having tandem differential stage. This is typically 10^4 times.

Large Signal Transistor Model

A large signal model for a transistor was given by Ebers and Moll in 1954. The model they presented was for a P-N-P transistor. The Ebers-Moll model shown here is for an N-P-N transistor (Figure 1).

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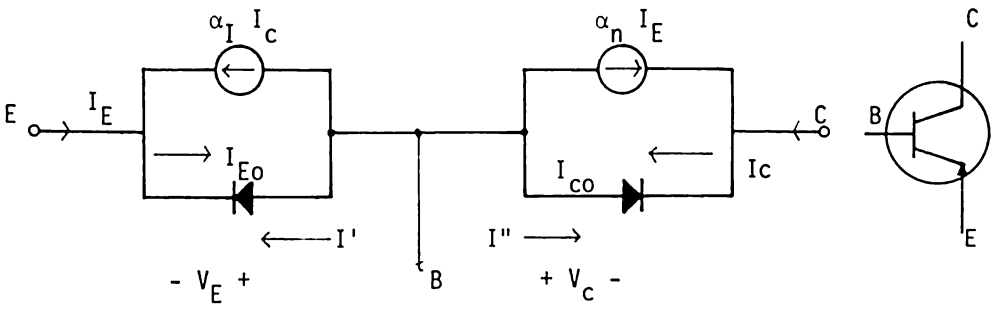


where

$$I' = I_{co}(E^{VE/VT} - 1),\quad I'' = 'Ico(E^{VC/VT} - 1),\quad V_T = \frac{KT}{q} \cong 26\,vm \text{ at } 27°$$

FIGURE I

α_I, α_N = Inverted and normal transport carrier ratio I_{CO}, I_{EO} = reverse saturation currents (typically $\sim 10^{-9}$ A for Si) ($\sim 10^{-6}$ A for Ge) the saturation currents I_{EO} and I_{CO} are related by:

$$\alpha_I I_{CO} = \alpha_N I_{EO}$$

Manufacturer's data sheets often provide information about $\alpha(=\alpha_N)$ I_{CO} and I_{EO} so that α_I may be determined. For many transistors, I_{EO} lies in the range 0.5 I_{CO} to I_{CO}. (1) We now replace the model in a typical circuit below. (Figure 2).

Active Region Model

If we bias a transistor in the active region we note that for an N-P-N, the collector base junction reversed bias and the base emitter junction is forward biased.

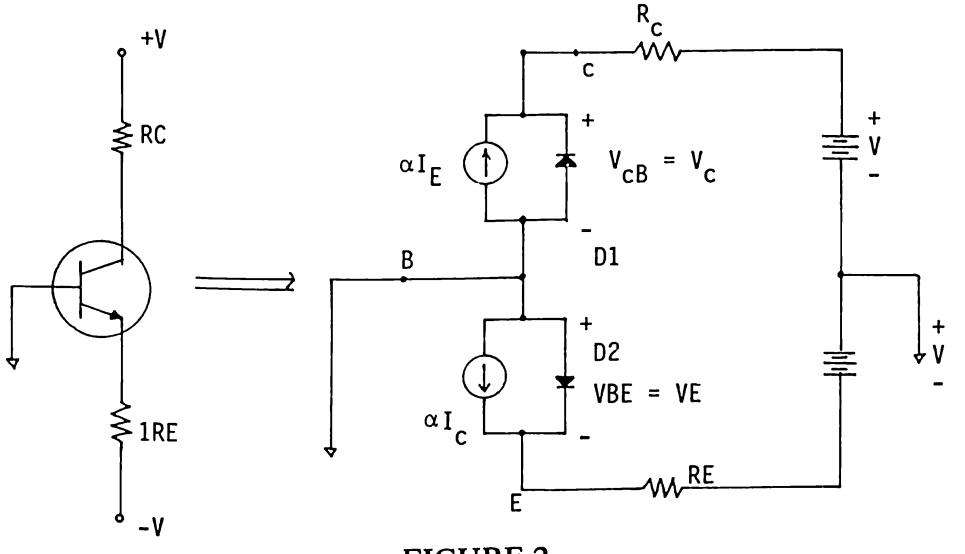
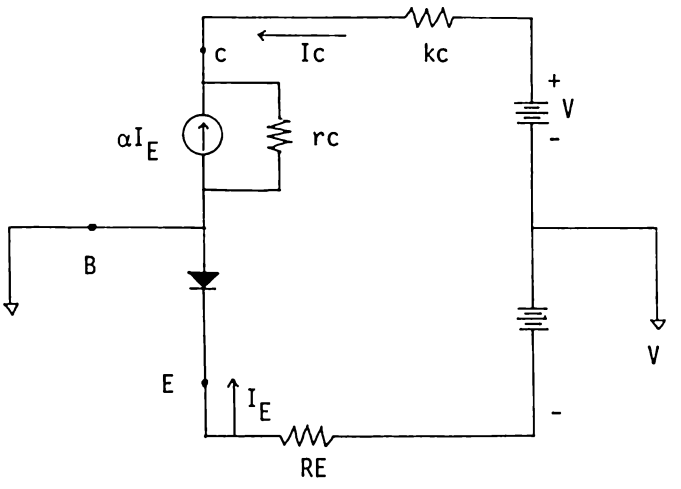


FIGURE 2

hence we could simplify the Eber's-Moll since D_1 is off and D_2 is on. We now simplify the model:



r_C = reverse resistance of D_1
tens of Meg ohms

FIGURE 3

From Figure 1 we solve for the current I_E:

$$I_E = -\alpha_I \; I_C - I' \qquad \text{EQ. A}$$

$$I_c = -\alpha_N \; I_E - I'' \qquad \text{EQ. B}$$

Substitute EQ. B into EQ. A.

$$I_E = -\alpha_I \; (-\alpha_N I_E - I'') - I'$$

$$I_E \; (1 - \alpha_I \; \alpha_N) = +\alpha_I I'' - I'$$

$$I_E = \frac{\alpha_I I'' - I'}{1 - \alpha I \; \alpha N}$$

Substituting for I' and I'' from equation defined in Figure 1:

$$I = \frac{\alpha I (I_{CO} \; (E^{VC/VT} - 1)) - I_{EO}(E^{VE/VT} - I)}{(1 - \alpha I \; \alpha N)}$$

Since Vc is the reverse bias voltage V_{CB} Vc $= -V_{CB}$ And since

$|V_c| >> V_T = 26mv$ the term $E^{-Vc/VT}$ drops out

Hence:

$$I_E \approx \frac{-\alpha_I I_{co} - I_{Eo}(E^{VE/VT} - 1)}{1 - \alpha 5\, \alpha N}$$

When the saturation current is small, I_{CO} drops out and $V_E >> V_T$, $E^{VE/VT}$ is large.

$$I_E \approx \frac{-I_{EO}(E^{VE/VT})}{1 - \alpha I\, \alpha N}$$

can simply be written as

$$I_E = -I_{ES}(E^{VE/VT}), \quad I_{ES} = \frac{I_{EO}}{1 - \alpha I\, \alpha N}$$

Small Signal Model

We note from the previous section that I is opposite the assumed direction thus 2 reversing I we can write Figure 4.

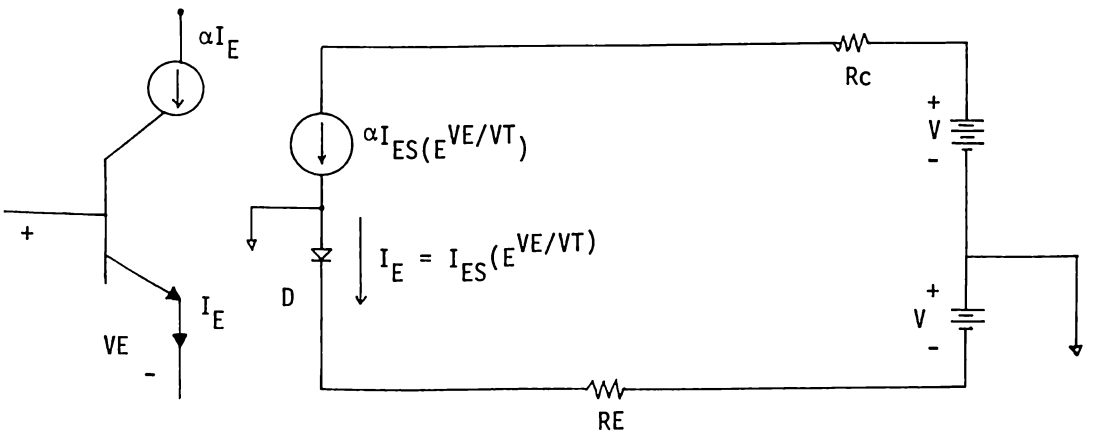


FIGURE 4

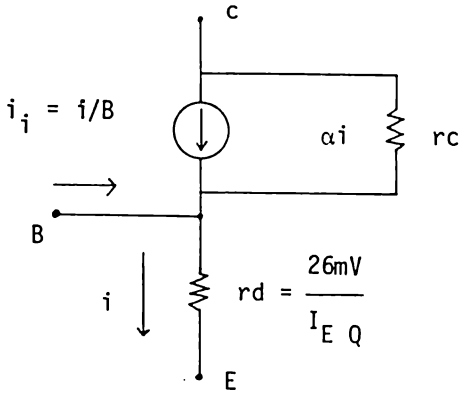
Linearize diode D: $I_E = I_{ES}\, \epsilon^{VE/VT}$

$$\frac{dI_E}{dV_E} = (I_{ES}\, E^{VE/VT}) \qquad \frac{1}{V_T} = \frac{I_E}{V_T} = Gm$$

or $r = \frac{1}{Gm} = \frac{V_T}{I_E} = \frac{26m\ V}{I_{EQ}}$ hence the dynamic resistance

where I_{EQ} = quiescent emitter current

depends on the emitter current. We could now form the small signal model suitable for small signal analysis.



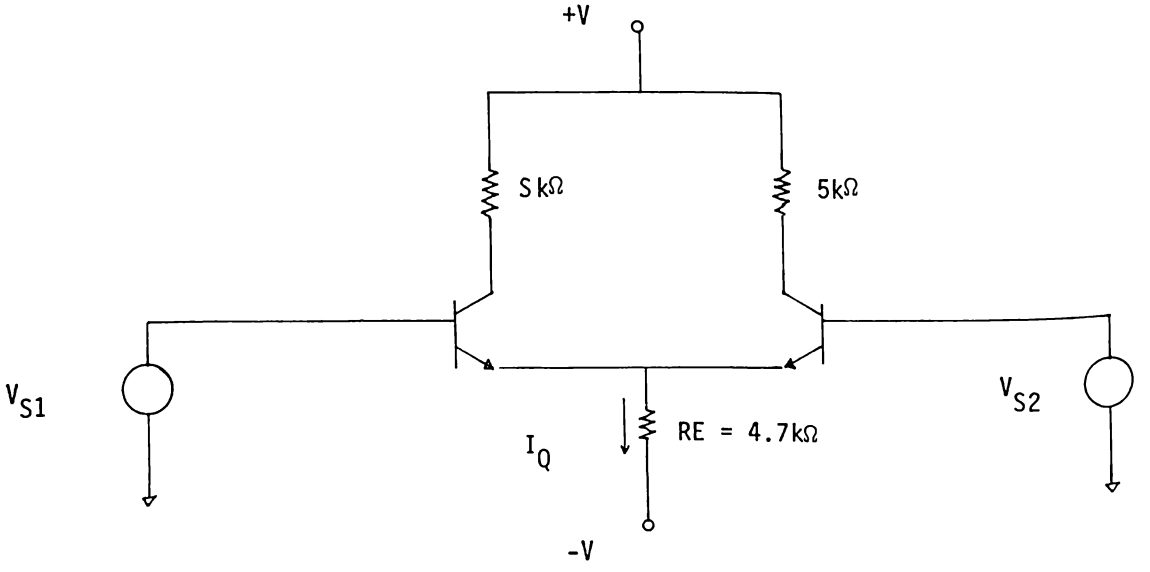
"T" transistor model

V_c is the reverse resistance of the diode D_1

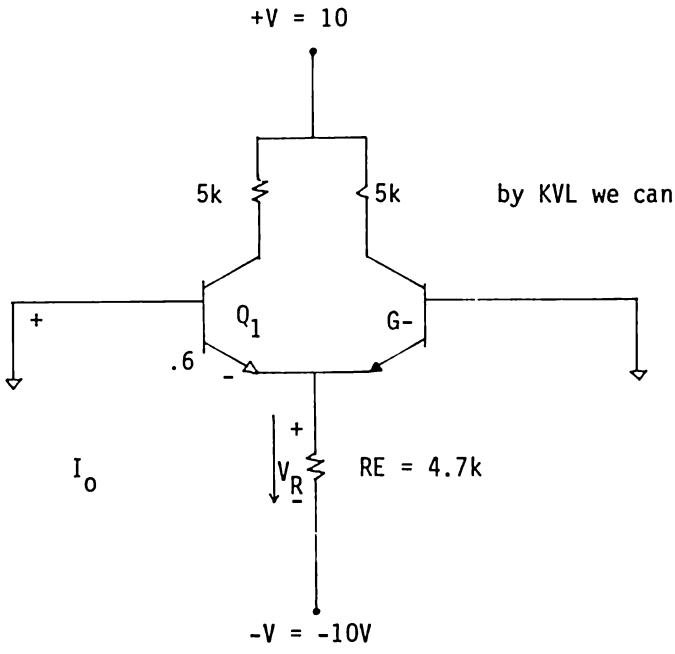
~ tens of Meg ohms

B = Common emitter current gain

Using the Model on A Differential Amplifier



DC analysis ckt:



$$I_o = \frac{V_R}{4.7k}$$

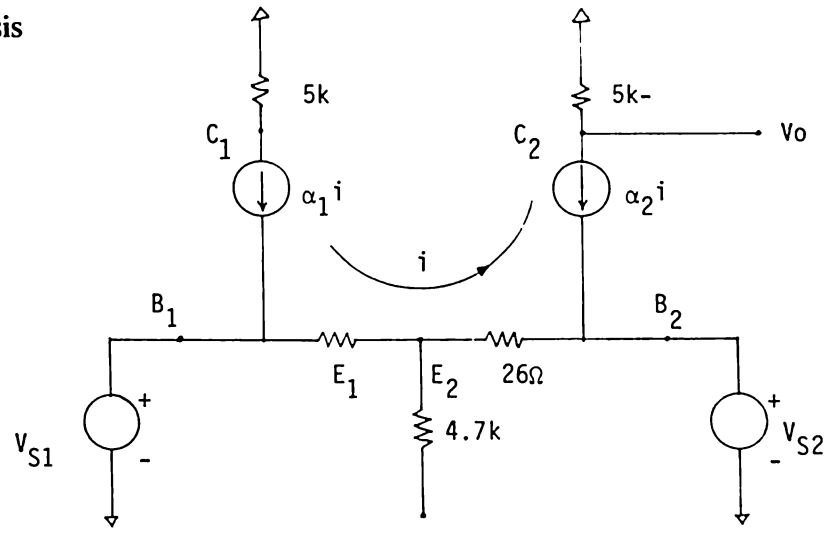
$$I_o \approx \frac{-0.6 - (-V)}{RE} = \frac{-.6 + 10}{4.7k} \approx 2 \text{ ma}$$

$$I_{E_{Q_1}} = I_{E_{Q_2}} = \frac{2ma}{2} = 1 \text{ ma.}$$

hence

$$d_1 = rd_2 = \frac{26 \text{ mV}}{1ma} = 26\Omega$$

AC analysis



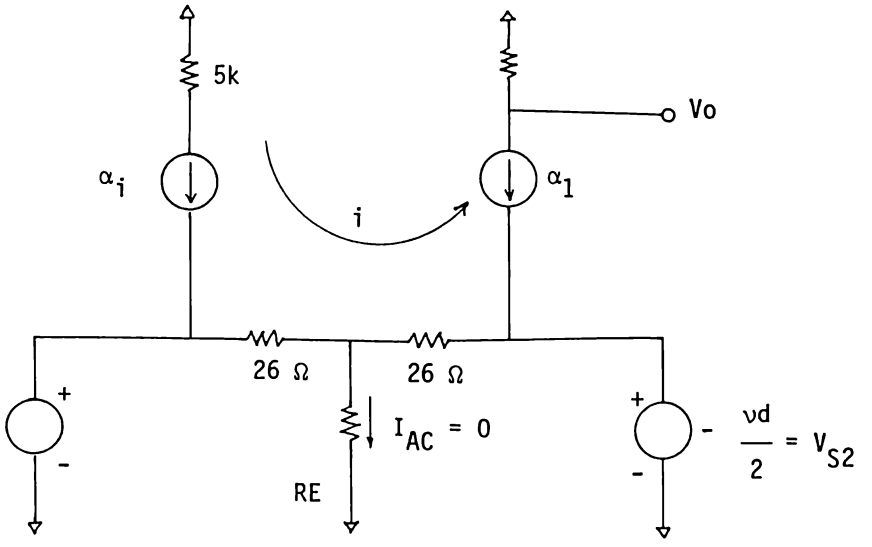
We can superpose V_{S1} and V_{S2} to look for Vo. However, we may define V_{S1} as equal to $Vc + \frac{Vd}{2}$ and V_{S2} as equal to $V_c - \frac{Vd}{2}$. Now, we superpose using the common mode voltage Vc and the differential mode voltage Vd.

Hence,

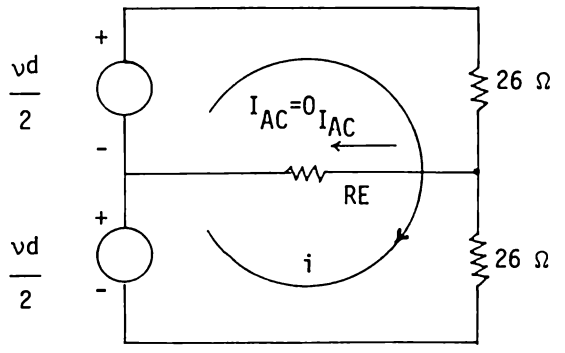
$$V_c = \frac{V_{Si} + V_{S2}}{2}, \quad Vo = V_{S1} - V_{S2}$$

Differential Mode Gain, Ad:

$$\text{Set } \nu c = 0 \quad \therefore V_{S1} = \frac{\nu d}{2}, \quad V_{S2} = -\frac{\nu d}{2}$$



Note $I_{AC} = 0$ since we have a balanced bridge:



Hence $Ad = \frac{Vc}{Vd} = ?$

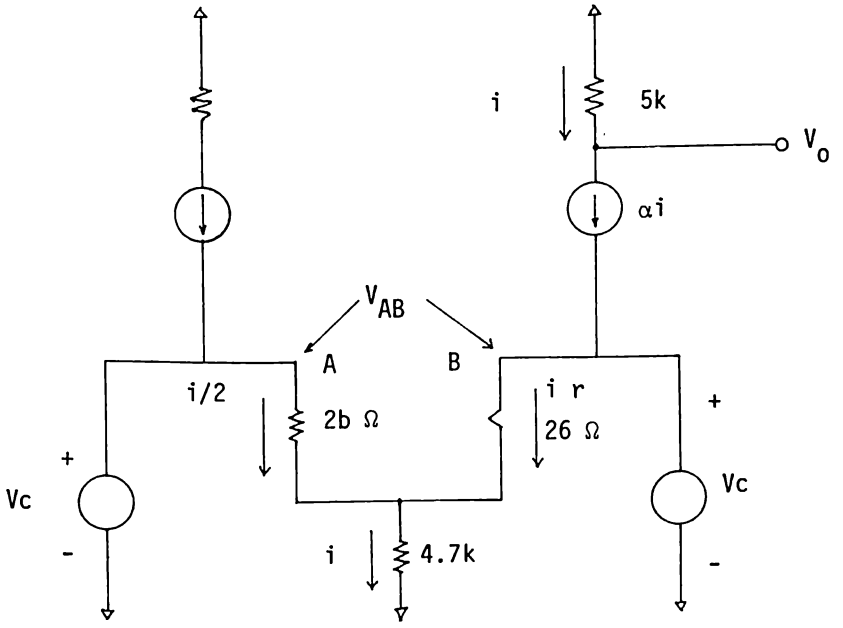
$$Vo = i5k,\ i = \frac{\frac{\nu d}{2} + \frac{Vd}{2}}{26 + 26} = \frac{\nu d}{(52)}$$

$$\therefore\ Ad = \frac{Vo}{\nu d} = \frac{5k}{Vd} = \frac{5k}{2(52)} = 96.2$$

$$\boxed{Ad = 96.2}$$

Common Mode Gain, AC:

Set $\nu d = 0$ $\quad\therefore\ V_{S1} = Vc\ ,\ V_{S2} = Vc$



By KVL, note V_{AB} = +Vc - Vc =) volts hence 26Ω are effectively in parallel

$$\text{:Hence } i = \frac{V_c}{4.7\text{ k} + (26 \,//\, 26)} = \frac{V_c}{4.713\text{k}}$$

$$Ac = \frac{\nu c}{\nu c} = ?$$

$$\nu o = -5\text{k } i/2$$

$$\therefore A_c = \frac{-5\text{k } (V_c / 4.713\text{k})/2}{V_c} = \frac{-5\text{k}/2}{4.713\text{k}} = -0.53$$

$$\boxed{Ac = -.53}$$

Both Modes:

$$Vo = Ad\nu d + Az\nu c$$

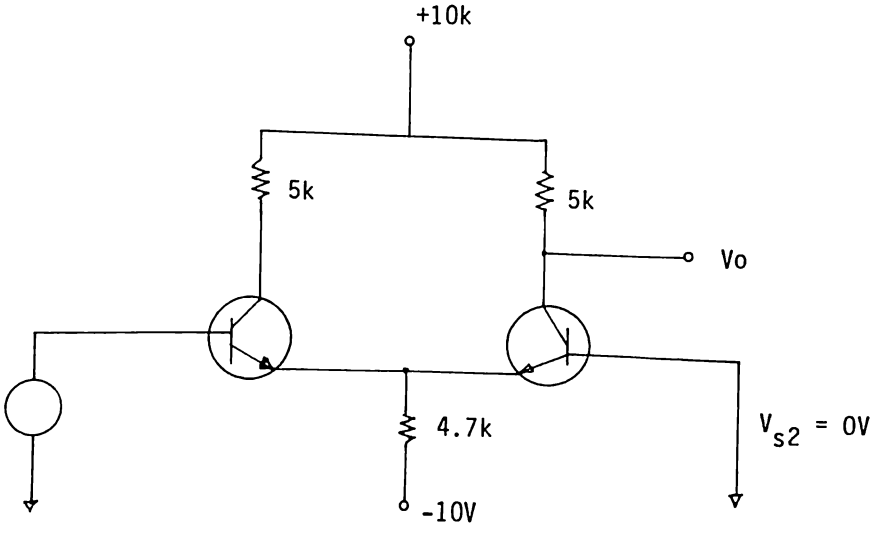
$$Vo = 96.2\ \nu d + (-.53)\ \nu c$$

$$Vo = 96.2\ \nu d\ \left(1 + \frac{-.53}{\frac{1}{CMRR}}\right) \nu c)$$

$$CMRR = \left| \frac{AD}{Ac} \right| = \left| \frac{96.2}{-.53} \right| = 182$$

$$CMRR = 20 \log |CMRR| = 20 \log 182 = \boxed{45.2 \text{ dB.}}$$

For Example



If V_{s1} = 10mvsin wt, Vo = ?

Thus

$$vd = V_{s1} - V_{s2} = V_{s1} 10m\nu \sin wt$$

$$vc = \frac{V_{s1} + V_{s2}}{2} = Vs1/2 = 5m\nu \sin wt$$

$$vo = Ad\ vd + Ac\ vc$$

$$vo = 96.2\ (10m\nu \sin wt) + (-.53)\ 5m\nu \sin wt$$

$$vo = 962m\nu \sin wt - 2.65m\nu \sin wt$$

$$\boxed{vo = 0.959 \sin wt}$$

Conclusion

The "T" transistor model was derived from the linearized Ebers-Moll active region assumption. Note the ease with which to analyze a differential amplifier using this particular model. In an experiment I have performed, the model is accurate to within 4% at best and 11% at worst case to the actual laboratory measurements.

References:

1. Electronics Devices and Circuits by
Millman & Halkias
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2. Electronic Circuits: Discrete & Integrated by
Schilling & Belone
McGraw Hill