High-Resolution Differential Thermography of Semiconductor Edifices

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ABSTRACT

We develop a cost-effective, high-resolution, and noninvasive imaging technique for thermal mapping of semiconductor edifices in integrated circuits. Initial implementation was done using a power-stabilized optical feedback laser system that detects changes in the optical beam-induced current when the package temperature of the device is increased. The linear change in detected current can be translated to a thermal gradient, which can reveal semiconductor "hotspots"—localized sites with anomalous thermal activity. These locales are possible fault sites or areas susceptible to defects, which are the best jump-off points for failure analysis.

INTRODUCTION

To perform successful failure analysis on a semiconductor device, precise knowledge of the exact fail site location is important. One of the most rapid ways to locate a fault zone is to uncover "hotspots"—edifices with temperatures above the accepted operating range of the device. Various hotspot isolation techniques have been in existence since the earliest days of failure analysis and have been satisfactory to varying degrees for the location of suspected damage sites on different integrated circuits.

Thermal imaging as a failure analysis tool has been implemented using infrared cameras (Rogalski, 2003) or array detectors (Christofferson et al., 2001). However, the high thermal discrimination and simple operation of these detectors are offset by the high purchase cost. Other detection techniques exist such as liquid-crystal microscopy (Lee & Pabbisetty, 1993) and scanning microscopy (Shi et al., 2003), but they are too invasive and less sensitive.

Aside from being expensive, all these methods solely detect remnants of thermal conduction bleeding through the surface of the integrated circuit. Because of their poor resolution in the axial direction, they cannot map out thermal propagation of an embedded defect. The challenge, therefore, is to develop a cost-effective, noninvasive thermographic technique that would enable us to localize and map out areas of high thermal gradient.

The method we propose will utilize a custom-built optical feedback microscope operating in the near-IR range (Cemine et al., 2004). The thermal response of the individual IC sections is then monitored and analyzed by measuring the optical beam-induced current (OBIC) as the package temperature is increased. Because longer wavelengths λ suffer less scattering ($\sim 1/\lambda^4$), the method can be used to noninvasively tunnel through thick layers of semiconductor die in contrast to the surface-limited probes of the scanning electron microscope (SEM) (Shi et al., 2004). High-resolution

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sample dissection can then be done as a verification procedure. Since there is no downtime for sample preparation, the analysis is simple, fast, and does not require a vacuum environment so essential to SEM imaging. This ease of maintenance is further supported by the system's simplification of the fault identification process: both defect localization and identification can be done in the same setup, cutting cost and experimental hours.

METHODOLOGY

A schematic diagram of the microscope setup is shown in Fig. 1. A semiconductor laser (SL) (Sharp LT024MD, λ = 793 nm at laser case temperature = 25°C) was used as a light source. It has a built-in photodetector (PD) that is used to detect the confocal reflectance signal. The SL is controlled by a laser diode controller that is connected to the computer. The diverging elliptical illumination beam was collimated by a collimating lens (C) (Melles Griot 06GLC003, numerical aperture = 0.276, focal length = 14.5 mm). Mounted anamorphic prisms (AP) (Melles Griot 06GPA004, magnification = 3x) were used to circularize the beam. An iris diaphragm (D) was inserted to lessen the effect of astigmatism.

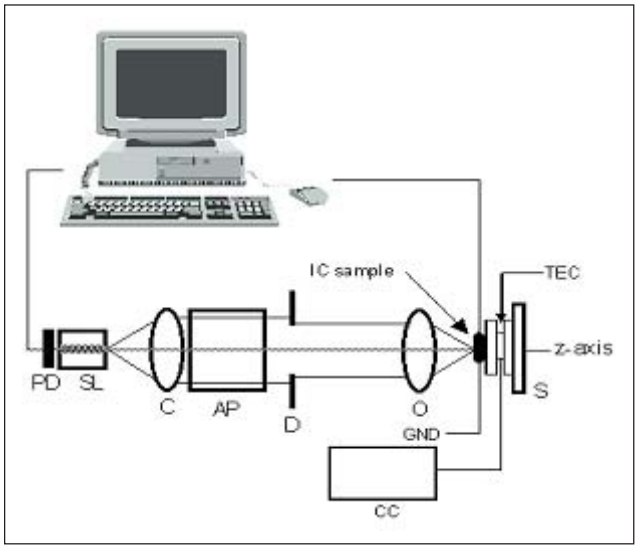

Fig. 1. Optical setup. Confocal and OBIC tandem microscope using an optical feedback laser system (SL). Collimating optics (C, AP) expand the beam which is focused by an objective (O) on the sample. The IC specimen is mounted on a thermoelectric cooler (TEC) to increase the package temperature by adjusting the current controller (CC).

An objective lens (O) (Olympus UPlan Fl, nominal NA = 0.5, working distance = 1.7 mm) was used to focus the beam on the sample. The current produced upon sample irradiation is the one-photon optical beam-induced current (1P-OBIC) signal. The light reflected from the sample forms the confocal reflectance signal. The sample is a photodiode array (MN8090 Matsushita 5017) biased at 3.56 V and is mounted on a triaxis servomotor stage (S) (Thorlabs PT3-Z6) that is controlled by a motion-controller card inside the computer. The sample is heated using a thermoelectric cooler (TEC) controlled by a current controller (CC), while the temperature is monitored using a multimeter.

Confocal reflectance and OBIC signals are detected using a 12-bit data-acquisition board (National Instruments 6024E, conversion rate = 200 kHz) inside the computer. Stage-scanning and image-acquisition protocols are coded using LabVIEW 7.0 (National Instruments).

Confocal and OBIC images were acquired for six sample temperatures: 25.1 (room temperature), 29, 38.2, 48.9, 61.6, and 72.1°C. The effect of the sample temperature on the OBIC signal generation is determined. OBIC thermal-gradient mapping of the sample image is undertaken to reveal die defects and sites that are susceptible to failure.

RESULTS AND DISCUSSION

Figure 2 shows the 190 mm x 190 mm 1P-OBIC and confocal reflectance images taken at the focus (Z = 0) for three sample temperatures: (a) 25.1, (b) 48.9, and (c) 72.1°C. For each measurement the object's axial location was monitored and adjusted to compensate for any package expansion that may have occurred. Identical confocal images mean that we are always investigating the same focal plane.

Notice the significant decrease in intensity on the OBIC image as temperature increases. This signifies that as the sample temperature increases, the current generated by the beam (the 1P-OBIC signal) at each point on the

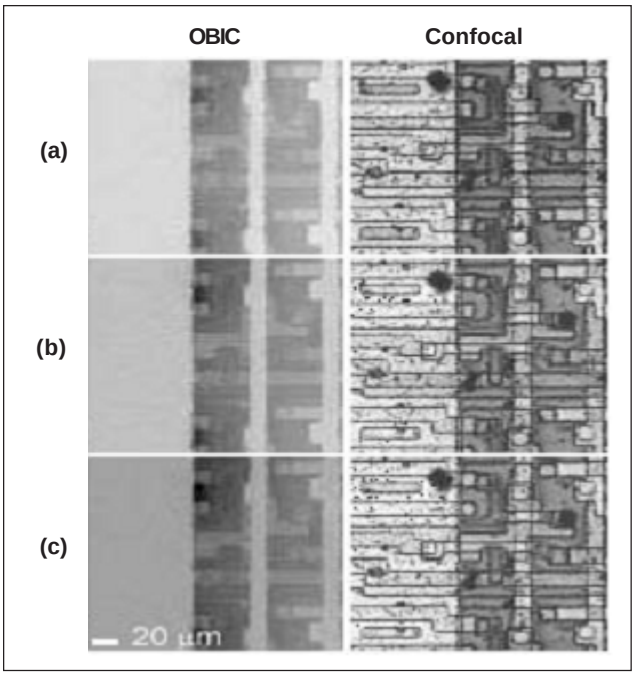

Fig. 2. The 190 mm x 190 mm confocal and 1P-OBIC images at (a) 25.1, (b) 48.9, and (c) 72.1ºC. OBIC intensity decreases as sample temperature increases.

observation area decreases. We operated the diode laser in power-stabilized mode ensuring a constant illumination power. The decrease in OBIC signal is then caused by the increase in resistance of the sample as the temperature of the sample increases. Quantification of this observed phenomenon will be presented later.

We determine the semiconductor and metal parts of our observation area by multiplying the OBIC and confocal images, and OBIC complement and confocal images, respectively. This method is already an established procedure for semiconductor and metal discrimination (Daria et al., 2002; Miranda & Saloma, 2003). As inputs, we use the OBIC and confocal images at room temperature (T =25.1°C). Figure 3 shows the confocal and OBIC images at room temperature and their corresponding semiconductor and metal sites. The portions that are low in intensity on both the semiconductor and metal images are either the dielectric or the substrate.

Five different portions (each of area 20 mm x 20 mm) on the OBIC images are selected to quantitatively determine the OBIC signal decrease as the temperature increases [Figs. 4(a) and 4(b)]. Figure 4(c) shows the

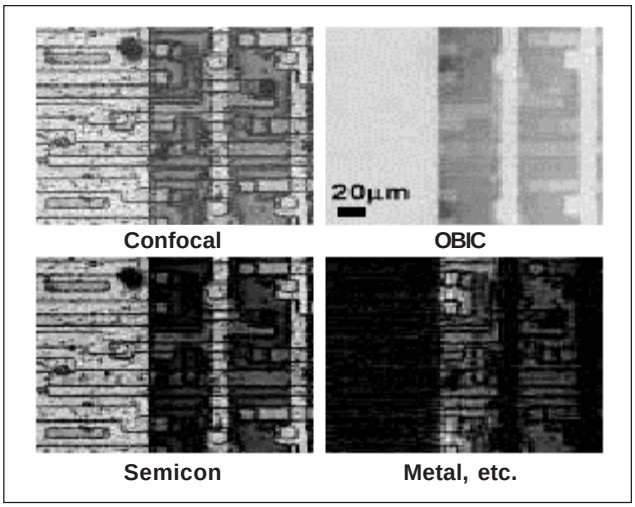

Fig. 3. Confocal and 1P-OBIC images for room temperature and their corresponding semiconductor and metal sites.

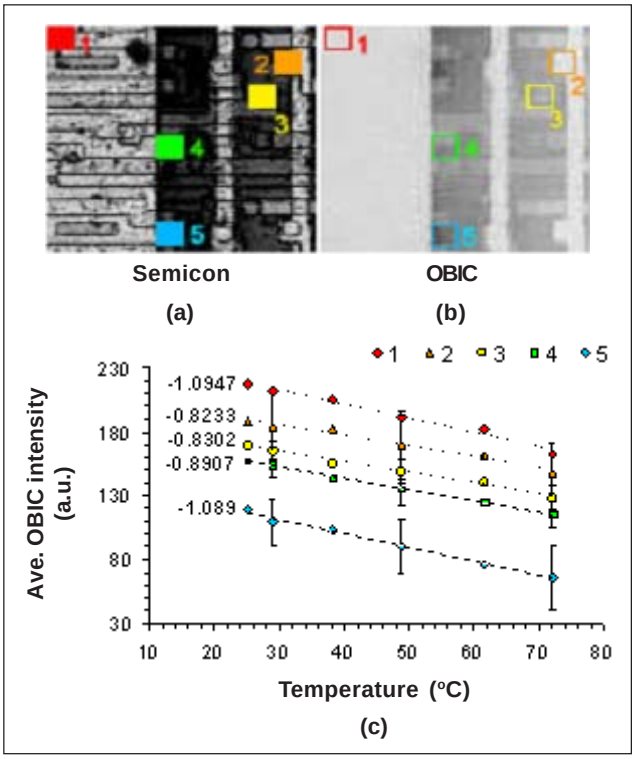

Fig. 4. [(a) and (b)] Semiconductor and OBIC images. (c) Average OBIC intensity of the five monitored sites decreases versus the temperature of the sample. The numbers are the slopes of the curves. Image size is 190 x 190 mm.

plots of the OBIC average intensities versus temperature for the five portions. Their respective slopes, which represent the OBIC signal rate of change with temperature, are also shown.

For the five portions, OBIC linearly decreases with temperature. However, the rate of decrease of the OBIC signal at these five regions are different, as exhibited by their differing slope values. This implies that some portions of the integrated circuit (IC) heat up faster than other areas. Those regions that heat up faster reflect a faster OBIC signal decrease or a steeper slope, while those that heat up slower exhibit a gradual decrease in OBIC signal. This inhomogeneity in heating rate can reveal the locations of those sites that are either defective or highly susceptible to failures when the IC is operated at extreme conditions.

We can map those defective and failure-susceptible sites by getting the thermal gradient map using the OBIC images for the six temperature levels. Figure 5 shows the thermal-gradient map of the observation area. Notice the thermal-gradient inhomogeneity on the observation area as exhibited by the different colors on the thermal-gradient map. Areas that heat up fast are reflected as red on the map (pointed by arrows), while areas that heat up slow are blue. From this observation, imaging and localization of those sites that are either defective or susceptible to defect, is realized.

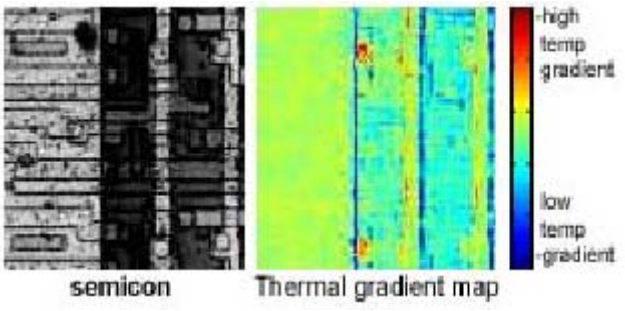

Figure 5. Semiconductor image and thermal gradient map of the sample. Red portions (pointed by arrows) indicate highest rate of change in temperature while blue portions indicate lowest rate of change in temperature.

CONCLUSION

We have demonstrated the performance of our newly developed noninvasive imaging technique for thermal mapping of semiconductor edifices in integrated circuits. The technique detects thermal-gradient inhomogeneity on the IC observation area. Those sites that heat up fast are well discriminated from those sites that heat up at a slower rate.

With this capability, our technique cannot only act as a failure analysis tool but can be used for precursor or predictive analysis as well. Possible defect sites can be mapped out even before failure happens. In such eventuality, the onset and evolution of a failure can be recorded and investigated. Semiconductor architecture can also possibly benefit from the technique by deriving thermal accumulation points in a particular semiconductor design. The technique can provide such basic tests to expose weaknesses in prototype integrated circuits under thermal stress.

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