

# Device Fabrication of 60 $\mu\text{m}$ Resonant Cavity Light-Emitting Diode

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## ABSTRACT

An array of 60-mm-diameter resonant cavity light-emitting diodes suited for coupling with fiber optic were fabricated using standard device fabrication technique. *I-V* characterization was used to determine the viability of the device fabricating process. Under forward bias, the turn-on voltage of the devices is 1.95–2.45 V with a series resistance of 17–14 kW. Under reverse bias, the devices showed a breakdown voltage of 35 V.

## INTRODUCTION

Laser diode and light-emitting diodes (LEDs) are effective light sources (Koudelka & Woodall, 2002) for optical communication system (Dumitrescu et al., 2002). For this purpose, VCSEL/RCE geometry structure (Dumitrescu et al., 2002) is better preferred over conventional laser and LED structure for its superior optical properties, which include higher spectral purity (Dumitrescu et al., 2002; Schubert et al., 1992), better directionality and coupling efficiency (Dumitrescu et al., 2002; Gökkavas et al., 2001; Corbett, 1993), high brightness, increased efficiency, and ease of fabricating two-dimensional arrays of devices (Dumitrescu et al., 2002). For many applications, like low-cost short-haul communication system (Dumitrescu et al., 2002; Schnitzer et al., 1993), resonant cavity LEDs (RCLEDs) emitting in the same red wavelength range offer a suitable alternative over VCSELs (Dumitrescu et al., 2002; Schnitzer et al., 1993) because of its thresholdless operation, better

thermal behavior, and robustness. While the geometry structure allows easy coupling with optic fibers, it is also desirable to have an active window size that is comparable to the fiber optics, which has typical core diameters of 50 and 62.5  $\mu\text{m}$  (Gökkavas et al., 2001).

The Condensed Matter Physics Laboratory of the National Institute of Physics, UP Diliman, is making an active participation in the development of optoelectronic devices that can be used for optoelectronics applications. In the past years, we were able to grow GaAs-based heterostructure semiconductor layers and fabricate them into devices. These devices include vertical cavity surface-emitting lasers (VCSELs) (Manasan et al., 2004; Samson et al., 2003; Estacio et al., 2003; Agra, 2003), edge-emitting lasers (Manasan et al., 2003), light-emitting diodes (LEDs) (Agra et al., 2004), and photodetectors (Somintac et al., 2001).

The VCSELs and LEDs that the CMPL had fabricated, 250  $\mu\text{m}$  device diameter, have relatively large active window compared with the size of the optical fiber. In

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this work, we designed a fabrication process for 60-mm-diameter RCLEDs that can be easily coupled with the typical fiber optic size. The challenge in the new design is to provide the device with a large enough  $p$  contact dimension (Fig. 2) for ease in interconnects. The thickness of the ring  $p$  contact is approximately 10 mm, which is relatively small for wire bonding. The solution is to add a top metal pad, which is made feasible by the addition of a polyimide overlay.

## EXPERIMENTAL METHOD

### Sample description

The sample used, a VCSEL/RCE  $p$ - $i$ - $n$  layer, was grown on  $n$ -type (001) GaAs substrate (Somintac et al., 2001) using a Riber 32-P molecular beam epitaxy (MBE). Figure 1 shows the schematic diagram of the layer structure grown. The sequence consists of a GaAs (1.0 mm) buffer layer followed by 28 pairs of silicon-doped AlAs (710 Å) and AlGaAs (623 Å) layers, three pairs of AlGaAs (60 Å) and GaAs (95 Å) quantum wells (QW), then 24 pairs of beryllium-doped AlAs (710 Å) and AlGaAs (623 Å) layers, and finally, a beryllium-doped GaAs (100 Å) cap layer.

### Device design

Figure 2 is the device structure design for a 60 mm device. In addition to the conventional device structure, polyimide is added as an overlay to make the deposition of a top pad contact possible.

### Device fabrication

Before the sample was fabricated into the 60 mm device, the indium on the backside was removed using an indium removal solution (10% ammonium hydroxide). The sample was then degreased using the standard degreasing procedure, which includes 2–5 min soak in TCE, acetone, and methanol baths with ultrasonic agitation. The sample was rinsed under free-flowing de-ionized (DI) water, then finally blown dry with high-purity nitrogen gas.

To fabricate the designed 60 mm device structure, the sample underwent the standard device fabrication

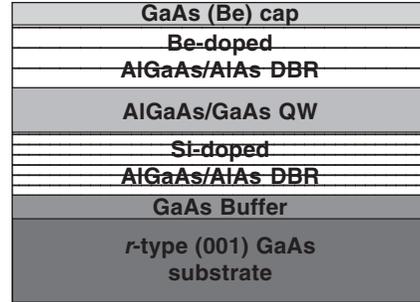


Fig. 1. Schematic diagram of VCSEL/RCE layer structure.

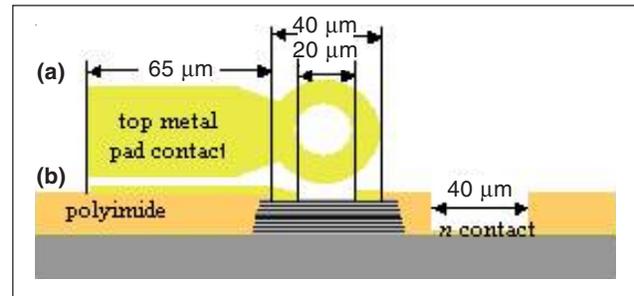


Fig. 2. Schematic diagram of the 60  $\mu\text{m}$  device structure showing dimensions. (a) Top view of the metal pad. (b) Side view of the device structure.

technique. This includes photolithography using the Karl Suss MJ3 mask aligner system, etching, and metallization processes. The summary of the fabrication process is shown in Fig. 3. Figure 3(a) is the prefabricated MBE sample. The ring contact was defined under UV exposure of the negative photoresist (ma-N 425<sub>B</sub>) [Figs. 3(b) and 3(c)], spin coated over the sample, using patterned mask. After developing, the top contact, AuZn/Ti/Au, was deposited using an in-house-built metallization setup. Photoresist was stripped off using acetone and the metal was alloyed [Fig. 3(d)] using a tube furnace with high-purity nitrogen purge. The 60 mm mesa was created by, initially, pattern definition of positive photoresist (ma-P 275) under UV exposure [Figs. 3(e) and 3(f)] and then etching [Fig. 3(g)] of the patterned sample using a  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (1:8:80) etchant solution. The pattern for the bottom contact was defined using UV exposure [Figs. 3(h) and 3(i)]. Afterwards, the bottom contact, AuGe/Ni/Au, was deposited, the photoresist was lifted off, and then the metal was alloyed [Fig. 3(j)]. To create the top metal pad, a polyimide overlay was added. An overlay pattern was defined using UV exposure [Figs. 3(k) and 3(l)] of a Durimide 7005

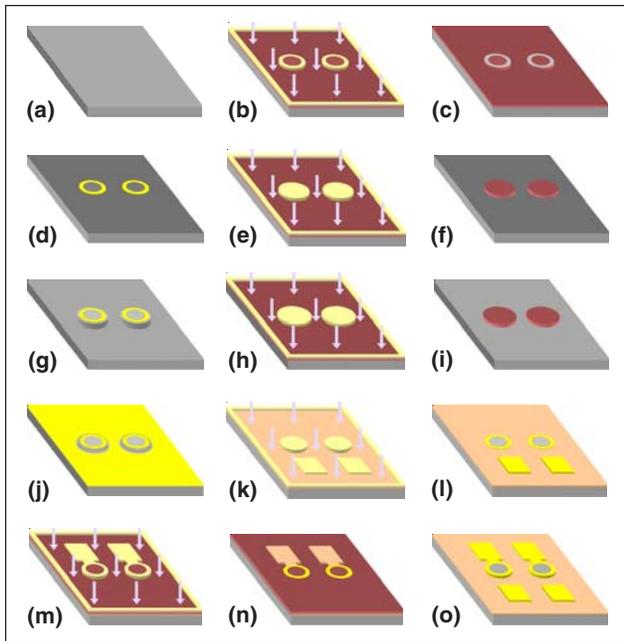


Fig. 3. Schematic diagram for fabrication of the 60  $\mu\text{m}$  device.

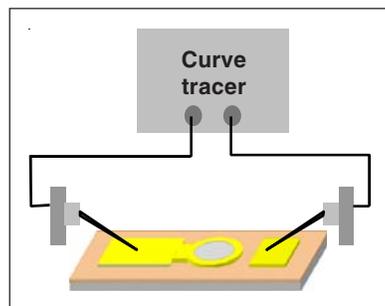


Fig. 4. Schematic diagram of  $I$ - $V$  characterization setup.

negative polyimide spin coated over the sample. An opening on the polyimide overlay was created next to the top and bottom contacts (Fig. 2). The top metal pad was deposited by, first, pattern definition using the photolithography process [Figs. 3(m) and 3(n)], then metal deposition, and finally, removal of the photoresist. The final device structure is shown in Figs. 2(b) and 3(o).

### Device characterization

Current-voltage ( $I$ - $V$ ) measurement, which gives information such as turn-on voltage and sample resistance, was used to check the viability of the 60  $\mu\text{m}$  device fabricated. The characterization setup used is shown in Fig. 4. The sample was mounted on a

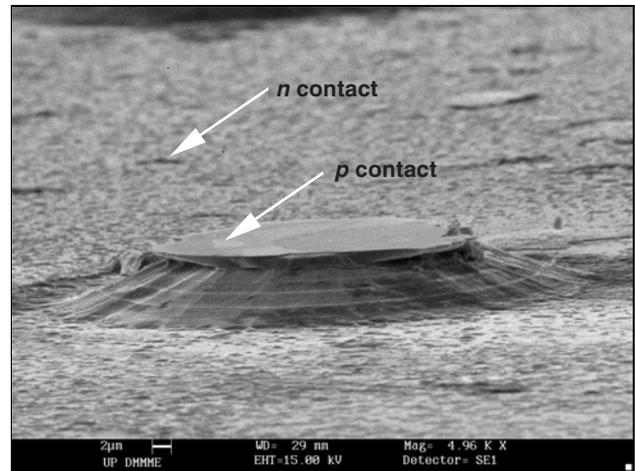


Fig. 5. SEM micrograph of the 60  $\mu\text{m}$  device structure (4.96K x magnification).

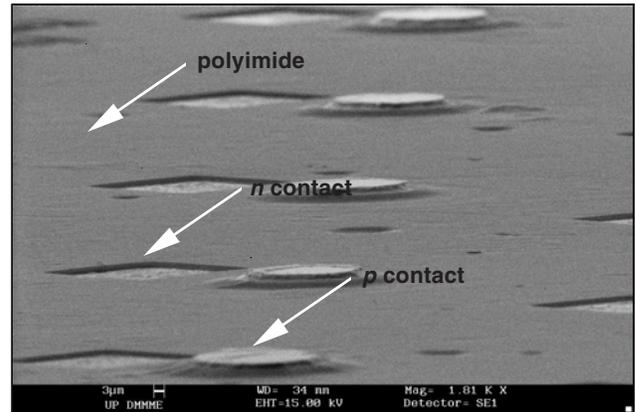


Fig. 6. Isometric view of polyimide overlay (1.81K x magnification).

needle-probe  $XYZ$  translation stage and the current-voltage ( $I$ - $V$ ) curves were taken using a Tektronix  $I$ - $V$  curve tracer.

## RESULTS AND DISCUSSION

Figure 5 is the SEM micrograph of a 60  $\mu\text{m}$  device in Fig. 3(j), showing a clearly defined layer profile of the sample. In Fig. 6 is the SEM micrograph of a 60  $\mu\text{m}$  device with a polyimide overlay, showing an opening next to the top and bottom contacts. Notice that the layer profile is completely covered with polyimide, which therefore prevents short circuit in the device. The micrograph of a complete 60  $\mu\text{m}$  device fabricated is shown in Fig. 7.

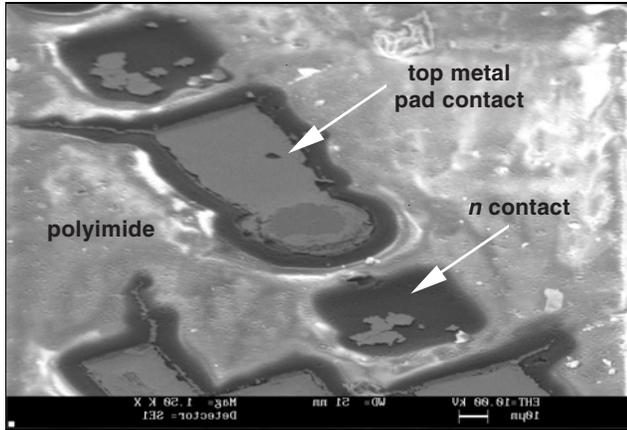


Fig. 7. Isometric view of the 60 μm device with polyimide overlay and top metal pad (1.5K x magnification).

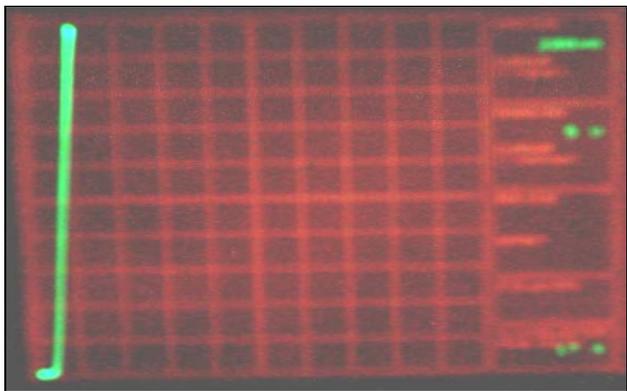


Fig. 9. *I-V* characteristic of the 250 mm RCLED (200 mA x 5 V).

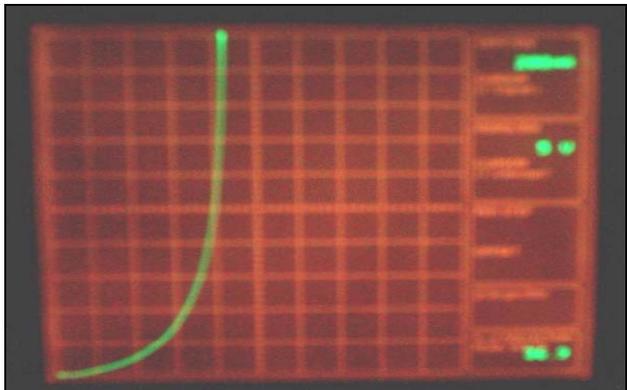


Fig. 8. *I-V* characteristic of the 60 mm RCLED (200 mA x 5 V).

The *I-V* characteristic of a 60 mm RCLED device is shown in Fig. 8. The curve shows an exponential behavior, which agrees with the diode equation,  $I = I_0 \exp[(eV/k_B T) - 1]$  (where  $I_0$  is the leakage current in

reverse bias,  $e$  is the electronic charge,  $V$  is the bias voltage,  $k_B$  is the Boltzman constant, and  $T$  is the absolute temperature). Under forward bias, the *I-V* characteristic shows a turn-on voltage at 1.95 V. At high forward bias, the current increase differs from exponential and shows linear *I-V* characteristics. This area exhibits a relatively low differential conductivity ( $dI/dV$ ) indicating a high device series resistance, around 6 kW. Under reverse bias, the sample shows a breakdown voltage of 35 V. Figure 9 is the *I-V* characteristic of a 250 mm RCLED device. The sample shows a turn-on voltage of 1.3 V and a series resistance of around 6 kW. Both devices of different dimensions have different turn-on voltages. This could be possible since the 60 mm device underwent numerous steps during device fabrication. A previous step may leave a residue on the surface of the device prior to metallization, which could be a possible cause of the device’s high resistance. Both devices show a high series resistance, which was initially attributed to the high resistance of DBR layers, but a non-DBR layer also shows a high series resistance of 4–8 kW. High resistance can then be attributed to alloying of the metal contact, since the alloying parameters were not optimized.

**CONCLUSION**

The SEM micrograph and the *I-V* curve demonstrated the viability the CMPL to fabricate small devices such as 60 mm RCLEDs. This represents a substantial improvement in our device fabrication capabilities. Further improvements in alloying for metal contact are needed to lower the device’s high series resistance.

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